



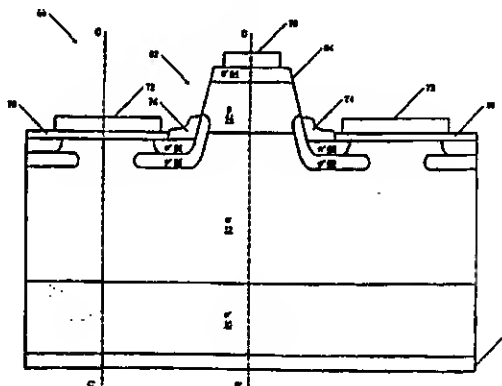
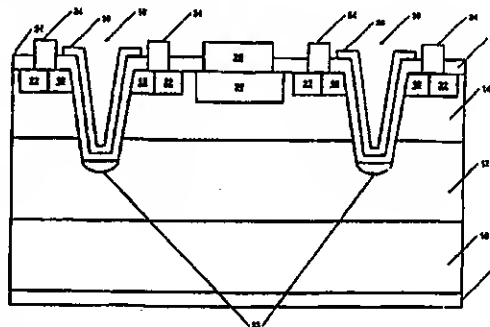
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(54) Title: LATCH-UP FREE POWER MOS-BIPOLAR TRANSISTOR

## (57) Abstract

A MOS bipolar transistor is provided which includes a silicon carbide npn bipolar transistor formed on a bulk single crystal n-type silicon carbide substrate and having an n-type drift layer and a p-type base layer. Preferably the base layer is formed by epitaxial growth and formed as a mesa. A silicon carbide nMOSFET is formed adjacent the npn bipolar transistor such that a voltage applied to the gate of the nMOSFET causes the npn bipolar transistor to enter a conductive state. The nMOSFET has a source and a drain formed so as to provide base current to the npn bipolar transistor when the bipolar transistor is in a conductive state. Also included are means for converting electron current flowing between the source and the drain into whole current for injection into the p-type base layer. Means for reducing field crowding associated with an insulating layer of said nMOSFET may also be provided.



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## LATCH-UP FREE POWER MOS-BIPOLAR TRANSISTOR

Related Application

The present application is a continuation of United States Patent Application Serial No. 08/891,221 filed July 10, 1997, which is related to and claims priority from United States Provisional Patent Application Serial No. 60/049,423, filed June 12, 1997 and entitled *LATCHUP-FREE POWER UMOS-BIPOLAR TRANSISTOR (LMBT)*.

Field of the Invention

10 The present invention relates to semiconductor devices and more particularly to such devices formed in silicon carbide. The present invention particularly relates to power transistors formed in silicon carbide.

15

Background of the Invention

The silicon bipolar transistor has been the device of choice for high power applications in motor drive circuits, appliance controls, robotics and lighting ballasts. This is because bipolar transistors can be designed to handle relatively large current densities in the range of 200 to 50 A/cm<sup>2</sup> and support relatively high blocking voltages in the range of 500-2500V.

25 Despite the attractive power ratings achieved by bipolar transistors, there exist several fundamental

drawbacks to their suitability for all high power applications. Bipolar transistors are current controlled devices which require relatively large base control currents, typically one fifth to one tenth of the collector current, to maintain the transistor in an on-state mode. Proportionally larger base currents can be expected for applications which also require high speed turn-off. Because of the large base current demands, the base drive circuitry for controlling turn-on and turn-off is relatively complex and expensive. Bipolar transistors are also vulnerable to premature breakdown if a high current and high voltage are simultaneously applied to the device, as commonly required in inductive power circuit applications. Furthermore, it is relatively difficult to operate bipolar transistors in parallel because current diversion to a single transistor typically occurs at high temperatures, making emitter ballasting schemes necessary. This current diversion generally results from the decrease in on-state voltage drop across the bipolar device with further increases in operating temperature.

The silicon power MOSFET was developed to address this base drive problem. In a power MOSFET, the gate electrode provides turn-on and turn-off control upon the application of an appropriate gate bias. For example, turn-on in an n-type enhancement MOSFET occurs when a conductive n-type inversion layer is formed in the p-type channel region in response to the application of a positive gate bias. The inversion layer electrically connects the n-type source and drain regions and allows for majority carrier conduction between source and drain.

The power MOSFET's gate electrode is separated from the conducting channel region by an intervening insulating layer, typically silicon dioxide. Because the gate is insulated from the

channel region, little gate current is required to maintain the MOSFET in a conductive state or to switch the MOSFET from an on-state to an off-state or vice-versa. The gate current is kept small during switching because the gate forms a capacitor with the MOSFET's channel region. Thus, only charging and discharging current ("displacement current") is required during switching. Because of the high input impedance associated with the insulated-gate electrode, minimal current demands are placed on the gate and the gate drive circuitry can be easily implemented.

Moreover, because current conduction in the MOSFET occurs through majority carrier transport only, the delay associated with the recombination of excess minority carriers is not present. Accordingly, the switching speed of power MOSFETs can be made orders of magnitude faster than that of bipolar transistors. Unlike bipolar transistors, power MOSFETs can be designed to simultaneously withstand high current densities and the application of high voltages for relatively long durations, without encountering the destructive failure mechanism known as "second breakdown". Power MOSFETs can also easily be paralleled, because the forward voltage drop of power MOSFETs increases with increasing temperature, thereby promoting an even current distribution in parallel connected devices.

The above-described beneficial characteristics of power MOSFETs are typically offset, however, by the relatively high on-resistance of the MOSFET's drift region for high voltage devices, which arises from the absence of minority carrier injection. As a result, a MOSFET's operating forward current density is typically limited to relatively low values, typically in the range of 40-50 A/cm<sup>2</sup>, for a 600 V device, as compared to 100-120 A/cm<sup>2</sup> for the bipolar transistor for an identical on-state voltage drop.

On the basis of these features of power bipolar transistors and MOSFET devices, devices embodying a combination of bipolar current conduction with MOS-controlled current flow were developed and found to provide significant advantages over single technologies such as bipolar or MOSFET alone. One example of a device which combines bipolar and MOS characteristics is the Insulated Gate Bipolar Transistor (IGBT).

The IGBT combines the high impedance gate of the power MOSFET with the small on-state conduction losses of the power bipolar transistor. Because of these features, the IGBT has been used extensively in inductive switching circuits, such as those required for motor control applications. These applications require devices having wide forward-biased safe-operating-area (FBSOA) and wide reverse-biased safe-operating-area (RBSOA).

One disadvantage of an IGBT is its limited gate control on-state current density. This arises from the presence of a parasitic thyristor in its structure. At sufficiently high on-state current densities, this thyristor latches up, thereby losing gate control over the on current. This characteristic of IGBT's also limits the IGBT's surge current capability. Many proposals have been made for mechanisms to suppress the effectiveness of this parasitic thyristor at the cost of on-state voltage drop and/or switching speed.

Recent efforts have also included investigation of the use of silicon carbide (SiC) devices for power devices. Such devices include power MOSFETs such as are described in United States Patent No. 5,506,421. Similarly, silicon carbide Junction Field Effect Transistors (JFETs) and Metal-Semiconductor Field Effect Transistors (MESFETs) have also been proposed for high power applications. See

United States Patent Nos. 5,264,713 and 5,270,554. These devices, however, have a forward voltage drop of approximately 3 volts as a minimum voltage drop. Thus, these devices are not suitable for all applications.

5           Silicon carbide IGBTs may further provide improved performance over other power devices because the forward voltage drop of the device does not increase with breakdown voltage at the same rate for an IGBT as for a MOSFET or JFET. As is illustrated in  
10   Figure 1, the curve of breakdown voltage (BV) versus forward voltage drop (Vf) for a MOSFET/JFET 8 crosses the curve for a silicon carbide IGBT 9 at about 2000V. Thus, for breakdown voltages of greater than 2000V silicon carbide IGBTs may provide better performance in  
15   terms of forward voltage drop for the same breakdown voltage than silicon MOSFETs or JFETs.

          While the characteristics of the silicon carbide IGBT indicate promise as a power device, such devices are currently limited in their applicability in  
20   silicon carbide. These limitations are a result of the present difficulties in fabricating good quality highly doped p-type silicon carbide substrates. Another limitation is the very low hole mobility in silicon carbide, thereby making it very susceptible to  
25   parasitic thyristor latch-up. Therefore, silicon carbide IGBTs are expected to have a low value of gate controlled on-state current density. Because the IGBT is typically a vertical device, the substrate on which the device is fabricated may be critical to device  
30   performance. The quality of the substrate material may be a limiting factor in the fabrication of quality devices. Thus, the difficulty in manufacturing good quality highly doped p-type silicon carbide substrates may presently limit the fabrication of IGBTs to n-type  
35   substrates.

          In conventional power circuits it is desirable to have a device which may have the control

voltage applied to the device to turn the device on and off referenced to ground rather than to a high positive voltage level. However, to provide an IGBT where the gate is referenced to the emitter of the device  
5 generally requires a highly doped p-type substrate. As is noted above, highly doped p-type substrates currently are more difficult to fabricate than n-type substrates in silicon carbide. With an n-type substrate a silicon carbide IGBT would have its gate voltage  
10 referenced to the collector voltage which, in a typical power circuit would be to a line voltage. Thus, present silicon carbide IGBTs may require more complex gate drive circuitry with level shifting components and result in more complex power circuits as a result of  
15 the structure of IGBTs, the electrical characteristics of silicon carbide and the limitations in fabrication of highly doped p-type silicon carbide substrates.

In light of the above discussion, there exists a need for improvements in high power silicon  
20 carbide devices.

#### Object and Summary of the Invention

In view of the foregoing, it is one object of the present invention to provide a silicon carbide  
25 power device.

A further object of the present invention is to provide a silicon carbide power device which is voltage controlled.

Yet another object of the present invention  
30 is to provide a silicon carbide power device which may have its control voltage referenced to ground in typical power circuits while the collector voltage is capable of blocking a positive high voltage.

Still another object of the present invention  
35 is to provide a silicon carbide power device which may be fabricated on an n-type silicon carbide substrate.



Another object of the present invention is to provide a bipolar transistor which may be paralleled with other bipolar transistors with reduced instability arising from the decreasing on-state voltage drop of bipolar transistors with an increase in operating temperature.

Yet another object of the present invention is to provide a silicon carbide power device with an increased breakdown voltage.

Another object of the present invention is to provide silicon carbide MOS control with reduced susceptibility to gate dielectric breakdown during reverse bias mode of operation.

These and other objects of the present invention are provided by a MOS bipolar transistor which includes a silicon carbide npn bipolar transistor formed on a bulk single crystal highly doped n-type silicon carbide substrate and having an n-type drift layer a p-type base layer. Preferably the base layer is formed by epitaxial growth and formed as a mesa. A silicon carbide nMOSFET is formed adjacent the npn bipolar transistor such that a voltage applied to the gate of the nMOSFET causes the npn bipolar transistor to enter a conductive state. The nMOSFET has a source and a drain formed so as to provide base current to the npn bipolar transistor when the bipolar transistor is in a conductive state. Also included are means for converting electron current flowing between the source and the drain of the MOSFET into hole current for injection into the p-type base layer of the npn transistor. Means for reducing field crowding associated with an insulating layer of said nMOSFET may also be provided. Preferably, the nMOSFET is an accumulation mode device.

In particular embodiments, the means for converting comprises a silicon carbide tunnel diode formed between the nMOSFET and the npn bipolar

transistor so as to convert electron current flowing through the nMOSFET into hole current for injection into the base layer of the npn bipolar transistor. In such an embodiment the silicon carbide nMOSFET has an n-type conductivity source region and the tunnel diode is formed by forming a region of p-type conductivity silicon carbide having a higher carrier concentration than the p-type base layer adjacent the n-type conductivity source region so as to form a conductive p-n tunnel junction between the source region and the p-type conductivity region.

In one embodiment of the present invention, the means for converting includes a region of p-type conductivity silicon carbide in the p-type base layer and having a higher carrier concentration than the p-type base layer and an electrically conductive strap for electrically connecting the n-type source region of the nMOSFET to the region of p-type conductivity silicon carbide. Furthermore, the means for reducing field crowing may include a region of p-type conductivity silicon carbide formed in the drift layer beneath and spaced apart from the insulating layer and extending to the base layer.

In an embodiment having a mesa for the base layer, the sidewalls of the mesa may include a step portion. In such a case, a region of p-type conductivity silicon carbide may be formed in the p-type base layer at the step portion and having a higher carrier concentration than the p-type base layer. An electrically conductive strap electrically connects the n-type source region of the nMOSFET to the region of p-type conductivity silicon carbide.

In still another embodiment, where the mesa has sloped sidewalls, the slope of the sidewalls provides a predefined doping profile associated with the means for reducing field crowding.

Through the utilization of a region of p-type silicon carbide formed in the drift layer in proximity to the gate of the nMOSFET field crowding in the area of the gate may be reduced, thus increasing the breakdown voltage of the MOSFET. The formation of this region of p-type conductivity material may be facilitated by the formation of the base layer as a mesa having sloped sidewalls. The slope of the sidewall may then cooperate with the implantation process to provide the desired doping profile. Furthermore, by forming the base layer as a mesa the base layer may be formed by epitaxial growth and without the defects which may be caused by ion implantation in a significant portion of the base layer. The damage in the ion implanted base layer may lead to low npn transistor gain which may result in a high on-state voltage drop.

In another embodiment, the means for converting includes a region of p-type conductivity silicon carbide formed in the p-type base layer and having a higher carrier concentration than the p-type base layer and forming an electrically conductive strap for electrically connecting the n-type source region of the nMOSFET to the region of p-type conductivity silicon carbide.

In particular embodiments of the present invention, the silicon carbide nMOSFET comprises a UMOSFET having a gate trench formed adjacent the npn bipolar transistor and having a source region formed so as to provide electrons to the means for converting and wherein the npn bipolar transistor comprises a vertical npn bipolar transistor. Furthermore, the MOS bipolar transistor may be formed of a plurality of unit cells so as to provide a plurality of electrically parallel npn bipolar transistors.

By forming a MOS gated bipolar transistor where the electron current flow in the MOS transistor

is converted to hole current flow for injection into the bipolar transistor as base current, a voltage controlled bipolar device is provided. Furthermore, because the bipolar device is an npn device the bipolar transistor may be formed on an n-type silicon carbide substrate. Thus, the disadvantages of using a p-type substrate may be overcome. Also, because the device is an npn bipolar device the emitter of the device may be grounded which allows the gate control to be referenced to ground. Thus, in power circuits, devices of the present invention may utilize a ground referenced control circuit.

Furthermore, because base current of the bipolar device is injected from a MOS inversion channel which uses n channel conduction, the impact of low electron inversion layer mobility of silicon carbide may be reduced. Also, the characteristics of the MOS transistor which supplies base current to the bipolar device may tend to stabilize operation of multiple paralleled bipolar devices. Thus, while on-state resistance of the bipolar device decreases with increased temperature, on-state resistance of the base drive MOS transistor increases with temperature. The increased resistance of the MOS base drive transistor results in reduced base current in the bipolar device which then results in reduced current flow through the bipolar transistor. Therefore, even if the on-state resistance of the bipolar transistor reduces with temperature the current through the transistor may be reduced because of the reduced base current supplied by the MOS transistor. This interaction may provide added benefit where devices according to the present invention are comprised of a unit cell which may be replicated to provide for multiple electrically parallel bipolar transistors in a single substrate to allow increased current capability.

Devices according to the present invention also have no possibility of latch-up. The present devices are latch-up free because no parasitic thyristor exists in the structure of the present invention in contrast to the structure of an IGBT.

Devices according to the present invention also provides a wide forward bias safe operating area because of the presence of current saturation mode. Also devices according to the present invention have a large reverse bias safe operating area because of the higher impact ionization rate of holes than electrons in 4H-SiC. These characteristics are especially suitable for inductive switching applications.

In addition to embodiments described above, the present invention also provides a unit cell of a UMOS bipolar transistor which includes an n-type bulk single crystal silicon carbide substrate and an n-type silicon carbide drift layer formed on the n-type conductivity bulk single crystal silicon carbide substrate. The n-type drift layer has a carrier concentration of less than the n-type silicon carbide substrate. A p-type silicon carbide base layer is formed on the n-type silicon carbide drift layer and a first region of n-type silicon carbide is formed in the p-type base layer. A gate trench is formed in the p-type base layer and extends through the base layer and a portion of the first region of n-type silicon carbide to the drift layer to provide a portion of the first n-type region as a portion of the sidewall of the gate trench. An insulating layer is formed on the bottom and sidewalls of the gate trench and a second region of n-type conductivity silicon carbide is formed in the base layer adjacent and disposed from the gate trench. A conductive gate contact is formed on the insulating layer and extending over a portion of the first n-type region. A collector contact is formed on a surface of the silicon carbide substrate opposite the drift layer.

A p-type region of silicon carbide is formed in the base layer and is disposed between the first n-type region and the second n-type region. The p-type region has a carrier concentration greater than the carrier concentration of the p-type base layer and is formed so as to provide a reservoir of holes that convert electron current flowing through the first n-type region into hole current for injection into said p-type base layer. Finally, an emitter contact is formed on the second n-type region of silicon carbide.

In particular embodiments, a second p-type region of silicon carbide formed in the n-type silicon carbide drift region at the bottom of the gate trench is also provided. This second p-type region preferably has a carrier concentration greater than the carrier concentration of the n-type drift layer.

In another embodiment, the first p-type region forms a p-n junction with the first n-type region so as to provide a tunnel diode. Alternatively, a conductive strap formed between the first n-type region and the p-type region may be provided to electrically connect the p-type region to the first n-type region.

In particular embodiments of the present invention, the p-type base layer has a thickness of from about 0.3  $\mu\text{m}$  to about 5  $\mu\text{m}$ . The n-type drift region may have a thickness of from about 3  $\mu\text{m}$  to about 500  $\mu\text{m}$ . The n-type drift region may also have a carrier concentration of from about  $1 \times 10^{12} \text{cm}^{-3}$  to about  $1 \times 10^{17} \text{cm}^{-3}$  and the p-type base layer may have a carrier concentration of from about  $1 \times 10^{16} \text{cm}^{-3}$  to about  $1 \times 10^{18} \text{cm}^{-3}$ .

In still another embodiment of the present invention, a MOS gated bipolar transistor is provided which includes a plurality of the unit cells according to the present invention.

The present invention also includes methods of forming the devices described above. These methods

have the further advantage of allowing for fabrication of devices according to the present invention on the same substrate as UMOSFET silicon carbide transistors. Thus, the present invention also includes methods which

5. include the steps of forming an n-type silicon carbide drift layer on an n-type bulk single crystal silicon carbide substrate and forming a p-type silicon carbide base layer on the n-type silicon carbide drift layer. Ions are implanted through a first masking layer so as

10 to form n-type regions of silicon carbide in the base layer to provide an emitter region and a drain region. Ions are also implanted through a second masking layer so as to form a p-type region of silicon carbide adjacent the source region. A trench is etched through

15 a portion of the n-type source region and through the base layer and into the drift layer so as provide a gate trench. An insulating layer is formed on exposed surfaces of the base layer and the trench and a conductive contact is formed and patterned in the

20 trench and on the base layer so as to provide a gate contact. A portion of the insulating layer is removed to expose the emitter region formed in the base layer and an emitter contact formed on the exposed emitter region. A source/collector contact is formed on a

25 surface of the silicon carbide substrate opposite the drift layer.

In another embodiment of the methods according to the present invention, the step of implanting through a masking layer is followed by the

30 step of annealing the resultant structure at a temperature of greater than about 1500 °C. The methods may also include forming a p-type silicon carbide region in the n-type drift layer below the bottom of the trench.

35 In another embodiment of the methods of the present invention, a portion of the n-type source region and the p-type region of higher carrier

concentration formed in the base layer are exposed and a conductive strap is formed on the exposed portions to electrically connect the n-type source region to the p-type region.

5 In still further embodiments of the present invention, a unit cell of a MOS bipolar transistor is provided having an n-type bulk single crystal silicon  
10 carbide substrate and an n-type silicon carbide drift layer adjacent the n-type conductivity bulk single crystal silicon carbide substrate. The n-type drift layer has a carrier concentration of less than the n-type silicon carbide substrate. A p-type epitaxial silicon carbide base layer is formed on the n-type  
15 silicon carbide drift layer and a first n-type region of silicon carbide is formed in the p-type base layer adjacent a surface opposite the n-type silicon carbide drift layer. The p-type epitaxial silicon carbide base layer is formed as a mesa having a sidewall which extends through the p-type epitaxial silicon carbide  
20 base layer and to the n-type drift layer.

An insulating layer is formed on the n-type drift layer adjacent and disposed from the sidewall and a second n-type conductivity region of silicon carbide is formed in the drift layer adjacent the sidewall of  
25 the mesa. The second-n-type conductivity region has a higher carrier concentration than said drift layer. A gate contact is formed on the insulating layer and extending over a portion of the first n-type region. A collector contact is formed on a surface of the silicon  
30 carbide substrate opposite the drift layer. A first p-type region of silicon carbide is formed in the base layer and a second p-type region is formed adjacent the second n-type conductivity region and extending into the n-type drift region below the second n-type  
35 conductivity region and below the gate contact. The p-type regions have a carrier concentration greater than the carrier concentration of the p-type epitaxial base



layer. The first p-type region is formed so as to convert electrons flowing through the first n-type region into holes for injection into the p-type base layer. A conductive strap is also formed at base of the sidewall so as to electrically connect the second n-type conductivity regions with the first p-type region of silicon carbide and an emitter contact is formed on the first n-type region of silicon carbide.

In a particular embodiment, the first and second regions of p-type silicon carbide comprise a continuous region of p-type silicon carbide formed in the base layer adjacent a sidewall of the mesa and the second n-type conductivity region and extending into and below the gate contact.

In a further embodiment, the sidewall has a slope of less than about 60 degrees. The slope of the sidewall may be selected so as to produce the p-type region of silicon carbide when p-type ions are implanted at a predetermined depth in the drift layer.

In a further embodiment, the sidewall comprises two sidewalls so as to provide a step in the sidewall of said mesa. In such a case, the first p-type region of silicon carbide includes a first p-type region of silicon carbide formed in the p-type epitaxial base layer adjacent the step and a second p-type region of silicon carbide formed in the n-type drift layer. The second p-type region is formed adjacent the second n-type conductivity region and extends from the n-type drift layer below the gate contact to the p-type base layer. The conductive strap connects the first p-type region with the second p-type region and the second n-type conductivity region.

The unit cell of particular embodiments of the present invention may also have the second p-type region formed so as to be exposed at a surface of the drift layer. In such a case, the conductive strap electrically connects the first p-type region with the

second p-type region and the second n-type region. Furthermore, an insulating layer may be formed on the sidewall of the mesa between the drift layer and the step and extending onto the step. The conducting strap  
5 may then be formed on the insulating layer.

In particular embodiments, the p-type base layer has a thickness of from about 0.3  $\mu\text{m}$  to about 5  $\mu\text{m}$ . The n-type drift region may also have a thickness of from about 3  $\mu\text{m}$  to about 500  $\mu\text{m}$ . The n-type drift  
10 region may have a carrier concentration of from about  $10^{12}$  to about  $10^{17} \text{ cm}^{-3}$  and the p-type epitaxial base layer a carrier concentration of from about  $10^{16}$  to about  $10^{18} \text{ cm}^{-3}$ . The p-type region may extend beneath the gate contact a distance of from about 3  $\mu\text{m}$  to about 12  
15  $\mu\text{m}$ . The second n-type conductivity region be formed in the n-type drift layer to a depth of from about 0.3  $\mu\text{m}$  to about 5  $\mu\text{m}$ .

In further embodiments, the insulating layer comprises an oxide layer. Also, a MOS gated bipolar  
20 transistor may be formed by a plurality of the unit cells of the present invention. Methods for providing unit cells and transistors according to the present invention are also provided.

The foregoing and other objects, advantages  
25 and features of the invention, and the manner in which the same are accomplished, will become more readily apparent upon consideration of the following detailed description of the invention taken in conjunction with the accompanying drawings, which illustrate preferred  
30 and exemplary embodiments, and wherein:

#### Description of the Drawings

Figure 1 is a graph of breakdown voltage versus forward voltage drop for silicon MOSFETs and  
35 JFETs and silicon carbide IGBTs;

Figure 2 is a cross sectional view of a plurality of unit cells of a power device according to the present invention;

Figure 3 is a cross sectional view of an alternative embodiment of a plurality of unit cells of a power device according to the present invention;

Figure 4A through Figure 4J are cross sectional views illustrating the fabrication of a power device according to the present invention;

Figure 5 is a cross sectional view of a plurality of unit cells of a power device according to an alternative embodiment of the present invention;

Figure 6 is a cross-sectional view of a plurality of unit cells of a power device according to a second alternative embodiment of the present invention;

Figure 7 is a cross-sectional view of a plurality of unit cells of a power device according to a third alternative embodiment of the present invention; and

Figure 8A through Figure 8H are cross sectional views illustrating the fabrication of a power device according to an alternative embodiment of the present invention.

#### Detailed Description of the Preferred Embodiments

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout. Furthermore, the various layers and

regions illustrated in the figures are illustrated schematically. As will also be appreciated by those of skill in the art, references herein to a layer formed "on" a substrate or other layer may refer to the layer  
5 formed directly on the substrate or other layer or on an intervening layer or layers formed on the substrate or other layer. As will also be appreciated by those of skill in the art, while the present invention is described with respect to layers, such layers may be  
10 formed epitaxially or by implantation. Accordingly, the present invention is not limited to the relative size and spacing illustrated in the accompanying figures.

Figure 2 illustrates one embodiment of the  
15 present invention. As seen in Figure 2, a combination of unit cells of a latch-up free power UMOS bipolar transistor (LMBT) are illustrated. A unit cell of the first embodiment the present invention is illustrated between the lines A-A' and B-B' of Figure 2. By  
20 mirroring this unit cell around both the A-A' line and the B-B' line devices of multiple unit cells may be produced. Figure 2 illustrates a portion of a multiple unit cell device. As will be appreciated by those of skill in the art, the unit cell of the present  
25 invention may also be utilized to make a single unit cell device. In such a case the regions 18 and 22 need only be produced on the emitter side of the trench 16.

The LMBT of the present invention includes a bulk single crystal silicon carbide substrate 10 of n-  
30 type conductivity silicon carbide. The substrate 10 has an upper surface and a lower surface opposite the upper surface. A first layer 12 of n-type conductivity silicon carbide may be formed on the upper surface of the substrate 10 to form an n' drift region.  
35 Alternatively, an n' substrate could have an n' region implanted in the lower surface of the substrate so as to provide n' and n' regions in the substrate. Thus, as

used herein references to the substrate and first layer refer to layers formed both on the substrate and in the substrate. The carrier concentration of the substrate 10 is higher than the carrier concentration of the first layer 12. Thus, the substrate may be referred to as an n<sup>+</sup> substrate. Sheet resistivities of less than 1  $\Omega$ -cm may be suitable for the substrate 10. Carrier concentrations of from about  $10^{12}$  cm<sup>-3</sup> to about  $10^{17}$  cm<sup>-3</sup> may be suitable for the first layer 12. The substrate may have a thickness of from about 100  $\mu$ m to about 500  $\mu$ m. The first layer 12 may have a thickness of from about 3  $\mu$ m to about 500  $\mu$ m.

Formed on the first layer 12 is a second layer 14 to provide a p-type base layer. The second layer 14 may be epitaxially grown or implanted in the first layer 12 and is formed of p-type conductivity silicon carbide which forms a p-type base layer for the device. Formed in the second layer 14 is region 20 of n<sup>+</sup> conductivity silicon carbide which forms the emitter of the device. Also formed in the second layer 14 are n<sup>+</sup> regions 18 and p<sup>+</sup> regions 22. The p<sup>+</sup> silicon carbide regions 22 are preferably formed adjacent n<sup>+</sup> regions 18 such that a conductive p-n tunnel junction is formed between n<sup>+</sup> regions 18 and p<sup>+</sup> regions 22. The n<sup>+</sup> regions 18 are formed such that they form a portion of the sidewall of the gate trench 16. The n<sup>+</sup> regions 18 form the drain region of a MOS transistor incorporated into the present device.

The p-type base layer 14 preferably has a carrier concentration of from about  $10^{16}$  cm<sup>-3</sup> to about  $10^{18}$  cm<sup>-3</sup> and a thickness of from about 0.3  $\mu$ m to about 5  $\mu$ m. The n<sup>+</sup> regions 18 preferably extend between from about 0.5  $\mu$ m to about 2  $\mu$ m away from the gate trench 16 and extend to a depth of from about 0.1  $\mu$ m to about 2  $\mu$ m. Carrier concentrations of greater than about  $10^{18}$

cm<sup>-3</sup> maybe suitable for the n<sup>+</sup> regions 18. Similarly, the p<sup>+</sup> regions 22 are preferably formed to a depth of from about 0.1  $\mu$ m to about 2  $\mu$ m and have a width of from about 0.1  $\mu$ m to about 2  $\mu$ m. Carrier concentrations of greater than about 10<sup>16</sup> cm<sup>-3</sup> are suitable for the p<sup>+</sup> regions 22. The p-type regions 22 are also preferably separated from the emitter region 20 by from about 0.5  $\mu$ m to about 4  $\mu$ m. The size and shape of the emitter region may be dependent on the desired characteristics of the bipolar portion of the present device.

The device illustrated in Figure 2 also includes a gate trench 16. The gate trench 16 is formed by forming a trench which extends downward through n<sup>+</sup> regions 18 and the second layer 14 and into the first layer 12. Thus the gate trench 16 has sidewalls and a bottom. An insulator layer 24, preferably an oxide layer, is formed on the sidewalls and bottom of the gate trench and extends onto the upper surface of the n<sup>+</sup> regions 18. This insulator layer 24 is preferably an oxide layer such as silicon dioxide, but may also be made of other materials such as silicon nitride, aluminum nitride or other insulator materials known to those of skill in the art. The width and depth of the gate trench 16 is dependent upon the desired electrical properties of the device.

Widths of from about 1  $\mu$ m to about 10  $\mu$ m may be utilized for the present invention. The depth of the gate trench should be sufficiently deep such that the upper surface of the insulator/oxide layer 24 formed on the bottom of the gate trench 16 is below the interface between the second layer 14 and the first layer 12. Furthermore, the thickness of the gate insulator 24 is preferably from about 100 Å to about 1  $\mu$ m, but may vary depending on the desired electrical properties of the transistor.

The device of Figure 2 also includes an optional region of p-type conductivity silicon carbide 32 formed in the first layer 12 below the gate trench 16. This region of p-type conductivity silicon carbide 32 has a higher carrier concentration than the second layer 12. Carrier concentrations of from about  $10^{16}$  cm<sup>-3</sup> to about  $10^{19}$  cm<sup>-3</sup> may be utilized.

An ohmic contact is formed on the lower surface of the substrate 10 to create a collector contact 30. A contact is also formed on the sidewalls and bottom of the gate trench 16 and extends onto the upper surface of the n<sup>+</sup> regions 18. This contact provides a gate contact for the device of Figure 2. Finally, an ohmic contact 28 is formed on the n<sup>+</sup> silicon carbide region 20 to provide an emitter contact for the device.

The gate trench 16 is illustrated as two trenches in Figure 2. However, as will be appreciated by those of skill in the art, the gate trench may have many differing shapes in the third dimension (the dimension into and out of the page in Figure 2). Thus, for example, the device illustrated in Figure 2 may be a substantially circular device where the gate trenches 16 are a single gate trench which substantially surrounds the emitter region 20 as, for example, in a hexagonal shaped device. Also, the gate trenches 16 may be two substantially parallel trenches where the gate contacts 26 formed in the gate trenches 16 are electrically connected in the third dimension. Thus, the three dimensional configuration of the devices according to the present invention may take many differing forms while still benefiting from the teachings of the present invention.

Figure 3 illustrates an alternative embodiment of the present invention. As seen in Figure 3, the structure of the device of Figure 2 also has a conductive strap 34 connecting the n<sup>+</sup> region 18 to the

p<sup>+</sup> region 22. In the device illustrated in Figure 3, there should not be a rectifying p-n junction formed between n<sup>+</sup> region 18 and p<sup>+</sup> region 22. As will be appreciated by those of skill in the art, the unit cell illustrated in Figure 2 is also present in Figure 3. Thus, a device comprising any number of unit cells may be produced according to the teachings of the present invention.

As will be appreciated by those of skill in the art, the present invention may form the unit cell for a power device such that a plurality of the cells of the device may be formed and operated in parallel to increase the current carrying capabilities of the device. In such a case the unit cell of the device illustrated in Figure 2 or Figure 3 may be replicated in a symmetrical fashion to produce multiple devices. In such a device the outer gate trenches which are at the periphery of the device need only have the n-type and p-type regions on the emitter side of the gate trench.

Fabrication of the devices described above with respect to Figures 2 and 3 will now be described with reference to Figure 4A through Figure 4J. In fabricating the device of Figure 2, as illustrated in Figure 4A, a thick n-type layer 12 is grown on the n<sup>+</sup> substrate 10 utilizing an epitaxial growth process such as that described in the United States Patent No. 4,912,064, the disclosure of which is incorporated herein by reference as if set forth fully. As discussed above, alternatively, an n<sup>+</sup> substrate may be utilized and an n<sup>+</sup> implant performed to provide the n<sup>+</sup> layer 10 and n<sup>+</sup> layer 12. As illustrated in Figure 4B, a second p-type layer 14 is epitaxially grown on the first n-type epitaxial layer 12. The n<sup>+</sup> regions 18 and 20 are then formed on the p-type layer 14. These n<sup>+</sup> regions 18 and 20 may be formed by ion implantation using a mask 40 as illustrated in Figure 4C.



As is illustrated in Figure 4D, the p-type regions 22 may be formed by ion implantation utilizing a mask 42. The mask 42 is preferably formed so as to position the p-type regions 22 adjacent the n-type regions 18 so as to form a conductive p-n tunnel junction between these regions. After formation of the p-type regions 22 and the n-type regions 18 and 20, the structure is annealed at a temperature greater than about 1500 °C to activate the implanted ions.

After annealing, the device may be edge terminated by etching a mesa surrounding the device. The mesa (not shown) may extend through the second layer 14 and the first layer 12 and into the substrate 10. Alternatively, the mesa may extend through the second layer 14 and into the first layer 12. In such a case, ions may be implanted in the exposed n<sup>-</sup> layer 12 to a depth of from about 100 Å to about 5 μm and to a distance of from about 5 μm to about 500 μm from the edge of the mesa. Carrier concentrations of from about  $5 \times 10^{15} \text{ cm}^{-3}$  to about  $1 \times 10^{17} \text{ cm}^{-3}$  may be utilized to form a low doped p-type region surrounding the mesa. In either case a passivation layer may then be formed on the exposed surfaces of the mesa (not shown). Such a passivation layer may be SiO<sub>2</sub> or other such suitable materials known to those of skill in the art.

After creation of the epitaxial structure, a mask 44 is formed on the structure to position the gate trench of the device. Such a mask is illustrated in Figure 4E. The gate trench 16 is formed by reactive ion etching through the p-type base layer 14 into the n-type drift layer 12. The gate trench 16 may be etched utilizing the reactive ion etching techniques described in United States Patent No. 4,981,551, the disclosure of which is incorporated herein by reference as if set forth fully.

As seen in Figure 4F, a p-type region 32 may optionally be ion implanted at the bottom of the gate

trench 16. This p-type region 32 at the bottom of the trench 16 may reduce field crowding at the corner of the gate trench and, thereby, increase breakdown voltage of the MOS portion of the device. This p' 5 implanted region 32 may be formed by a method such as those described in United States Patent No. 5,087,576, the disclosure of which is incorporated herein by reference as if set forth fully.

After formation of the gate trench 16, an 10 insulator/oxide layer 26 is formed on the epitaxial structure as illustrated in Figure 4G. The insulator layer 24 is formed so as to cover the bottom and sidewalls of the trench 16 and extend onto the upper surface of the n' regions 18. The insulator/oxide layer 15 24 preferably utilizes either a thermal oxidation process such as that described in commonly assigned United States Patent Application Serial No. 08/554,319 entitled "Process For Reducing Defects In Oxide Layers In Silicon Carbide", the disclosure of which is 20 incorporated herein by reference as if set forth fully, or a deposited oxide process such as that described in United States Patent No. 5,459,107 and United States Patent Application Serial No. 08/554,319, the disclosures of which are incorporated herein by 25 reference as if set forth fully. If the thermal oxidation process is used then the preferred embodiment is to use carbon faced wafers such as described in United States Patent No. 5,506,421, the disclosure of which is incorporated herein by reference as if set 30 forth fully.

The formation of contacts for the present device is illustrated in Figures 4H through 4J. The gate contact may be formed by depositing a conducting layer in the gate trench 16 as illustrated in Figure 35 4H. As illustrated in Figure 4H the gate material 26, preferably molybdenum, may be deposited on the insulating layer 24 and patterned so as to extend above

a portion of the n-type region 18. As seen in Figure 4I, the emitter contact 28 and the optional conductive strap 34 may be formed simultaneously by forming openings in the insulating layer 24 and then depositing nickel or other suitable contact materials on the exposed portion of layer 14. Finally, as illustrated in Figure 4J, a collector contact 30 is formed on the exposed side of the substrate by deposition of nickel or other suitable contact material.

In each of the embodiments described above, the substrate and layers may be formed of silicon carbide selected from the group of 6H, 4H, 15R, or 3C silicon carbide, however, 4H silicon carbide is preferred for each of the devices described above. The preferred metals for ohmic contacts include nickel, tantalum silicide and platinum. Additionally, aluminum/titanium contacts may also be used to form the ohmic contacts of the present invention. While these particular metals have been described, any other metals known to those of skill in the art which form ohmic contacts with silicon carbide may be used.

With regard to the carrier concentrations or doping levels of the epitaxial layers and implanted regions of the devices described above, the p<sup>+</sup> or n<sup>+</sup> conductivity type regions and epitaxial layers should be as heavily doped as possible without causing excessive fabrication defects. Suitable dopants for producing the p-type regions include aluminum, boron or gallium. Suitable dopants for producing the n-type regions include nitrogen and phosphorus. Aluminum is the preferred dopant for the p<sup>+</sup> regions and it is preferred that the aluminum be implanted in the p<sup>+</sup> regions using high temperature ion implantation such as is described above and employing temperatures of between about 1000°C and about 1500°C. Carrier concentrations of up to about  $3 \times 10^{17} \text{ cm}^{-3}$  are suitable for the n epitaxial layers, however, carrier

concentrations of about  $3 \times 10^{16} \text{ cm}^{-3}$  or less are preferred.

As will be appreciated by those of skill in the art, the thickness of epitaxial layers 12 and 14 will be dependent upon the desired operating characteristics of the device. Furthermore, these operating characteristics will be affected by the number of unit cells employed and the geometry of the unit cells in a multiple cell device. The width of the gate trench will also be dependent upon the desired operating characteristics of the device, the number of unit cells employed to achieve those operating characteristics, and the geometry utilized for the unit cell itself.

In operation, the device of the present invention provides a silicon carbide device which combines bipolar conduction with MOS gated control. Furthermore, the present invention utilizes an n-type silicon carbide substrate which allows for referencing the gate voltage to the emitter of the device. This relationship allows for referencing the gate voltage to ground in a power circuit. Another advantage of the present invention is that n channel conduction through the MOS transistor is utilized for base current injection which reduces the impact of lower electron channel mobility in silicon carbide.

Turn on of devices according to the present invention is accomplished by the application of a positive bias on the collector 30 (about 3-10 V) and a positive bias on the gate 26 (about 15-40 V) while the emitter 28 is kept at ground potential. The source of the NMOSFET 18 is floating during the off state and is at approximately 3 V (the silicon carbide forward bias voltage drop for a p-n junction) above the emitter voltage in operation. A positive bias on the gate 26 enables the turn-on of the nMOSFET. The gate voltage ( $V_g$ ) for turn-on of the device will then be  $15\text{V} + V_t +$

3V, where  $V_t$  is the threshold voltage for the MOS device. Positively biasing the gate with respect to the source allows a path for the flow of electrons from the collector to the base of the npn transistor thereby forward biasing its emitter-base junction. The device achieves a high current density operation by the injection of minority carriers into the low doped drift region by the turn-on of the npn transistor. Hence, this device achieves a high current density with relatively low forward voltage drop. The base current to the npn transistor is limited by the saturation current of the MOS transistor which in turn results in current saturation characteristics of the LMBT. Higher gate voltage allows for higher base current into the npn transistor and hence a higher saturation current of the LMBT.

The device enters the forward blocking mode of operation when the gate potential is made the same as the emitter potential. This turns off the NMOSFET which reduces the base current of the npn transistor to zero. After the minority carriers of the npn transistor decay with their characteristic lifetime, the device stops carrying current and can support substantial collector voltage. This voltage is supported by the p-base 14 to n<sup>-</sup> drift region 12 junction and the p<sup>+</sup> buffer/gate oxide-n<sup>-</sup> drift region junction. The p<sup>+</sup> buffer region 32 may optionally be shorted to the p-base in the third dimension. The purpose of this buffer is to prevent high electric fields in the gate dielectric in the forward blocking mode of operation of the device.

Figure 5 illustrates an alternative embodiment of the present invention which utilizes an epitaxially formed p-type conductivity base region of the bipolar transistor and a buried p-type silicon carbide region to control the electric field presented to the gate insulator/oxide. As seen in Figure 5, a

combination of unit cells of a latch-up free power MOS bipolar transistor 60 are illustrated. A unit cell of the alternative embodiment the present invention is illustrated between the lines C-C' and D-D' of Figure 5. By mirroring this unit cell around both the C-C' line and the D-D' line devices of multiple unit cells may be produced. Figure 5 illustrates a portion of a multiple unit cell device. As will be appreciated by those of skill in the art, the unit cell of the present invention may also be utilized to make a single unit cell device.

As is seen in Figure 5, the MOS-Bipolar transistor 60 of the alternative embodiment of the present invention includes a bulk single crystal silicon carbide substrate 10 of n-type conductivity silicon carbide. The substrate 10 has an upper surface and a lower surface opposite the upper surface. A first layer 12 of n-type conductivity silicon carbide may be formed on the upper surface of the substrate 10 to form an n' drift region. Alternatively, an n' substrate could have an n' region implanted in the lower surface of the substrate so as to provide n' and n' regions in the substrate. Thus, as used herein references to the substrate and first layer refer to layers formed both on the substrate and in the substrate. The carrier concentration of the substrate 10 is higher than the carrier concentration of the first layer 12. Thus, the substrate may be referred to as an n' substrate. Sheet resistivities of less than 1  $\Omega$ -cm may be suitable for the substrate 10. Carrier concentrations of from about  $10^{12}$  cm<sup>-3</sup> to about  $10^{17}$  cm<sup>-3</sup> may be suitable for the first layer 12. The substrate may have a thickness of from about 100  $\mu$ m to about 500  $\mu$ m. The first layer 12 may have a thickness of from about 3  $\mu$ m to about 500  $\mu$ m.

Formed on the first layer 12 is a second layer 14 to provide a p-type base layer. The second layer 14 is preferably epitaxially grown and is formed

of p-type conductivity silicon carbide which forms a p-type base layer for the device. As is illustrated in Figure 5, the epitaxial layer 14 is patterned so as to form a mesa having a sidewall 62 which extends into the n layer 12. The sidewall 62 preferably extends into layer 12 as little as possible but depths of about 0.5  $\mu\text{m}$  may be acceptable. Preferably the sidewall of the mesa is sloped such that the base of the mesa is wider than the top of the mesa. This slope is preferably less than 60 degrees as measured by the angle the sidewall makes with the drift layer 12. Preferably the difference between the width of the top of mesa 62 and the width of the base of mesa 62 is less than about 10  $\mu\text{m}$ . However, this distance may vary depending on the thickness of the p-type base layer 14 and the first region of n-type silicon carbide 64 so as to achieve the desired slope of the sidewall of the mesa 62. The slope of the sidewall is preferably selected so as to cooperate with the implantation of atoms such that the profile of the p-type region 68 is formed. The slope facilitates implantation of the p-type regions 68 by allowing implantation of the p-type atoms such that the p-type region 68 extends to contact the p base layer 14. Thus, the slope of the mesa should be selected so as to provide a continuous region of implanted atoms which extend from the drift layer 12 to the base layer 14.

The MOS-bipolar transistor of the embodiment of the present invention illustrated in Figure 5 also includes a first region of n-type silicon carbide 64 formed on the p-type base layer 14 adjacent a surface opposite the n-type silicon carbide drift layer 12 to provide an emitter region for the bipolar transistor of the MOS-bipolar transistor 60. This first region of n-type silicon carbide 64 is preferably doped to have a higher carrier concentration than the n-type conductivity layer 12 so as to provide a first region

64 of n<sup>+</sup> silicon carbide. An ohmic contact is also formed on the first region of n-type silicon carbide 64 so as to provide an emitter contact 28.

5 An insulating layer 70 is formed on the first layer 12 adjacent to and disposed from the sidewall of the mesa 62. An ohmic contact is formed on the insulating layer 70 to provide a gate contact 72 for the MOS transistor. This insulator layer 70 is preferably an oxide layer such as silicon dioxide, but 10 may also be made of other materials such as silicon nitride, aluminum nitride or other insulator materials known to those of skill in the art.

The MOS-bipolar transistor 60 also includes a second region of n<sup>+</sup> silicon carbide 66 formed in the n<sup>+</sup> drift layer 12 at the base of the sidewall of mesa 62. 15 The n<sup>+</sup> region 66 extends from the sidewall of the mesa 62 to beneath a gate contact 72 of the device. The second region of n<sup>+</sup> silicon carbide 66 preferably is doped to provide a carrier concentration of greater 20 than the n<sup>+</sup> drift layer 12. The second region of n<sup>+</sup> silicon carbide 66 also preferably is formed adjacent the surface of the drift layer 12 so as to allow for contact between the second region of n<sup>+</sup> silicon carbide 66 and conductive strap 74.

25 A p-type region of silicon carbide 68 is also formed in the p-type base layer 14 adjacent a sidewall of mesa 62 and the second region of n<sup>+</sup> silicon carbide 66. The p-type region of silicon carbide 68 also extends in the n-type drift layer 12 below the second 30 region of n<sup>+</sup> silicon carbide 66 and extends below the gate contact 72. The p-type region of silicon carbide 68 is preferably doped to provide a carrier concentration greater than the carrier concentration of the p-type base layer 14. Furthermore, the p-type 35 region of silicon carbide is formed so as to convert electrons flowing through the second region of n<sup>+</sup> silicon carbide 66 into holes for injection in the p-



type base layer. The p-type region of silicon carbide 68 is also formed so as to reduce the field crowding associated with the gate insulator 70 to thereby increase the blocking voltage of the MOS transistor portion of the MOS-bipolar transistor 60.

The MOS-bipolar transistor 60 also includes a conductive strap 74 which electrically connects the second region of n' silicon carbide 66 with the p-type region of silicon carbide 68. Alternatively, the need for a conductive strap 74 may be eliminated if the p-n junction between the second region of n' silicon carbide 66 and the p-type region of silicon carbide forms a tunnel diode to thereby convert electron flow to hole flow in the base layer 14.

The p-type base layer 14 preferably has a carrier concentration of from about  $10^{16} \text{ cm}^{-3}$  to about  $10^{18} \text{ cm}^{-3}$  and a thickness of from about  $0.3 \text{ }\mu\text{m}$  to about  $5 \text{ }\mu\text{m}$ . The second n' regions 66 are preferably from about  $1 \text{ }\mu\text{m}$  to about  $5 \text{ }\mu\text{m}$  wide and extend under the gate as little as possible but this distance may range from about  $0.5 \text{ }\mu\text{m}$  to about  $3 \text{ }\mu\text{m}$ . The second n' regions 66 also preferably extend to a depth of from about  $0.1 \text{ }\mu\text{m}$  to about  $0.5 \text{ }\mu\text{m}$ . Carrier concentrations of greater than about  $10^{18} \text{ cm}^{-3}$  maybe suitable for the n' regions 66.

The p' regions 68 are preferably of a thickness of from about  $0.3 \text{ }\mu\text{m}$  to about  $2 \text{ }\mu\text{m}$  and extend beneath the gate contact 72 from about  $3 \text{ }\mu\text{m}$  to about  $12 \text{ }\mu\text{m}$ . However, the distance which the p' regions 68 extend beneath the gate contact may vary depending on the particular application. In particular, the space between p' regions 68 beneath a gate contact may be utilized to adjust the electric field near the insulating layer 70. As the space between p+ regions 68 decreases the electric field near the insulating

layer 70 may be reduced. Spacings of from about 1  $\mu\text{m}$  to about 5  $\mu\text{m}$  may be suitable. Carrier concentrations of greater than about  $10^{16} \text{ cm}^{-3}$  are suitable for the p' region 68. Preferably the doping of the drift layer 12 and p' region 68 are selected such that the drift layer 12 is completely depleted by the built-in potentials of the p'/n junction and the MOS gate at a zero gate bias.

Figure 6 illustrates a second alternative embodiment of the present invention which utilizes an epitaxially formed p-type conductivity base region of the bipolar transistor where the base region is formed as a mesa having a step in the sidewall of the mesa. As seen in Figure 6, a combination of unit cells of a latch-up free power MOS bipolar transistor 80 are illustrated. A unit cell of the alternative embodiment of the present invention is illustrated between the lines E-E' and F-F' of Figure 6. By mirroring this unit cell around both the E-E' line and the F-F' line devices of multiple unit cells may be produced. Figure 6 illustrates a portion of a multiple unit cell device. As will be appreciated by those of skill in the art, the unit cell of the present invention may also be utilized to make a single unit cell device.

As is seen in Figure 6, the MOS-Bipolar transistor 80 of the alternative embodiment of the present invention includes a bulk single crystal silicon carbide substrate 10 of n-type conductivity silicon carbide and a first layer 12 of n-type conductivity silicon carbide as is described with respect to Figure 5.

Formed on the first layer 12 is a second layer 14 to provide a p-type base layer. The second layer 14 is preferably epitaxially grown and is formed of p-type conductivity silicon carbide and forms a p-type base layer for the device. As is illustrated in Figure 6, the epitaxial layer 14 is patterned so as to form a mesa 82 having a sidewall which forms a step 84

and which extends to n<sup>+</sup> layer 12. The sidewall 82 preferably extends into layer 12 as little as possible but depths of about 0.5  $\mu\text{m}$  may be acceptable.

Preferably the sidewall of the mesa 82 which extends  
5 from the step 84 to the drift layer 12 is sloped such that the base of the mesa is wider than the width of the mesa at the step 84. This slope is preferably less than 60 degrees as measured by the angle the sidewall makes with the drift layer 12. Preferably the  
10 difference between the width of the top of mesa 82 and the width of the base of mesa 82 is less than about 10  $\mu\text{m}$ . However, this distance may vary depending on the thickness of the p-type base layer 14 and the first region of n-type silicon carbide 64 so as to achieve  
15 the desired slope of the sidewall of the mesa 82. Furthermore, the slope of the sidewall from the step portion 84 to the drift layer 12 is preferably selected so to cooperate with the implantation of atoms such that the profile of the p-type region 88 is formed.  
20 The slope facilitates implantation of the p-type regions 88 by allowing implantation of the p-type atoms such that the p-type region 88 extends to contact the p base layer 14. Thus, the slope of the mesa should be selected so as to provide a continuous region of  
25 implanted atoms which extend from the drift layer 12 to the base layer 14.

The MOS-bipolar transistor of the embodiment of the present invention illustrated in Figure 6 also includes a first region of n-type silicon carbide 64  
30 formed on the p-type base layer 14 adjacent a surface opposite the n-type silicon carbide drift layer 12 to provide an emitter region for the bipolar transistor of the MOS-bipolar transistor 80. This first region of n-type silicon carbide 64 is preferably doped to have a  
35 higher carrier concentration than the n-type conductivity layer 12 so as to provide a first region 64 of n<sup>+</sup> silicon carbide. An ohmic contact is also

formed on the first region of n-type silicon carbide 64 so as to provide an emitter contact 28.

An insulating layer 70 is formed on the first layer 12 adjacent to and disposed from the sidewall of the mesa 82. An ohmic contact is formed on the insulating layer 70 to provide a gate contact 72 for the MOS transistor. This insulator layer 70 is preferably an oxide layer such as silicon dioxide, but may also be made of other materials such as silicon nitride, aluminum nitride or other insulator materials known to those of skill in the art.

The MOS-bipolar transistor 80 also includes a second region of n<sup>+</sup> silicon carbide 86 formed in the n<sup>+</sup> drift layer 12 at the base of the sidewall of mesa 82 and extends from the sidewall to beneath a gate contact 72 of the device. The second region of n<sup>+</sup> silicon carbide 86 preferably is doped to provide a carrier concentration of greater than the n<sup>+</sup> drift layer 12. The second region of n<sup>+</sup> silicon carbide 86 also preferably is formed adjacent the surface of the drift layer 12 so as to allow for contact between the second region of n<sup>+</sup> silicon carbide 86 and conductive strap 92.

Regions of p-type silicon carbide 88 and 90 are also formed in the p-type base layer 14 adjacent second region of n<sup>+</sup> silicon carbide 86 and in the p-type base layer 14 at the step 84 in the mesa 82. The p-type region of silicon carbide 88 extends into the n<sup>+</sup> type drift layer 12 below the second region of n<sup>+</sup> silicon carbide 86 below the gate contact 72. The p-type regions of silicon carbide 88 and 90 are preferably doped to provide a carrier concentration greater than the carrier concentration of the p-type base layer 14. Furthermore, the p-type region of silicon carbide 90 is formed so as to convert electrons flowing through the second region of n<sup>+</sup> silicon carbide 86 into holes for injection in the p-type base layer. The p-type region of silicon carbide 88 is formed so as

to reduce the field crowding associated with the gate insulator 70 to thereby increase the blocking voltage of the MOS transistor portion of the MOS-bipolar transistor 80. The MOS-bipolar transistor 80 also includes a conductive strap 74 which electrically connects the second region of n<sup>+</sup> silicon carbide 86 with the p-type region of silicon carbide 90. The conductive strap 74 may also connect the second region of n<sup>+</sup> silicon carbide 86 with the p-type base layer 14 so as to place the p-type region 88 at the same potential as the second region of n<sup>+</sup> silicon carbide 86.

The p-type base layer 14 preferably has a carrier concentration of from about  $10^{16}$  cm<sup>-3</sup> to about  $10^{18}$  cm<sup>-3</sup> and a thickness of from about 0.3  $\mu$ m to about 5  $\mu$ m. The second n<sup>+</sup> regions 86 are preferably from about 1  $\mu$ m to about 5  $\mu$ m wide and extend under the gate as little as possible but this distance may range from about 0.5  $\mu$ m to about 3  $\mu$ m. The second n<sup>+</sup> regions 86 also preferably extend to a depth of from about 0.1  $\mu$ m to about 0.5  $\mu$ m. Carrier concentrations of greater than about  $10^{18}$  cm<sup>-3</sup> maybe suitable for the n<sup>+</sup> regions 86.

The p<sup>+</sup> regions 88 and 90 are preferably of a thickness of from about 0.3  $\mu$ m to about 2  $\mu$ m with region 88 extending beneath the gate contact 72 from about 3  $\mu$ m to about 12  $\mu$ m. However, the distance which the p<sup>+</sup> region 88 extends beneath the gate contact may vary depending on the particular application. In particular, the space between p<sup>+</sup> regions 88 beneath a gate contact may be utilized to adjust the electric field near the insulating layer 70. As the space between p<sup>+</sup> regions 88 decreases the electric field near the insulating layer 70 may be reduced. Spacings of from about 1  $\mu$ m to about 5  $\mu$ m may be suitable. Carrier concentrations of greater than about  $10^{16}$  cm<sup>-3</sup> are

suitable for the p<sup>+</sup> region 88 and 90. Preferably the doping of the drift layer 12 and p<sup>+</sup> region 88 is selected such that the drift layer 12 is completely depleted by the built-in potentials of the p<sup>+</sup>/n junction and the MOS gate at a zero gate bias.

Figure 7 illustrates a third alternative embodiment of the present invention which utilizes an epitaxially formed p-type conductivity base region of the bipolar transistor where the base region is formed as a mesa having a step in the sidewall of the mesa similar to that of Figure 6. As seen in Figure 7, a combination of unit cells of a latch-up free power MOS bipolar transistor 200 are illustrated. A unit cell of the alternative embodiment of the present invention is illustrated between the lines G-G' and H-H' of Figure 7. By mirroring this unit cell around both the G-G' line and the H-H' line devices of multiple unit cells may be produced. Figure 7 illustrates a portion of a multiple unit cell device. As will be appreciated by those of skill in the art, the unit cell of the present invention may also be utilized to make a single unit cell device.

As is seen in Figure 7, the MOS-Bipolar transistor 200 of the alternative embodiment of the present invention includes a bulk single crystal silicon carbide substrate 10 of n-type conductivity silicon carbide and a first layer 12 of n-type conductivity silicon carbide as is described with respect to Figures 5 and 6.

Formed on the first layer 12 is a second layer 14 to provide a p-type base layer. The second layer 14 is preferably epitaxially grown and is formed of p-type conductivity silicon carbide and forms a p-type base layer for the device. As is illustrated in Figure 7, the epitaxial layer 14 is patterned so as to form a mesa 282 having a sidewall which forms a step 284 and which extends to n<sup>-</sup> layer 12. The sidewall of

mesa 282 preferably extends into layer 12 as little as possible but depths of about 0.5  $\mu\text{m}$  may be acceptable. While the sidewall of the mesa 282 which extends from the step 284 to the drift layer 12 is illustrated as  
5 sloped such that the base of the mesa is wider than the width of the mesa at the step 284. However, such a slope is not required by the embodiment of the present invention illustrated in Figure 7.

The MOS-bipolar transistor of the embodiment  
10 of the present invention illustrated in Figure 7 also includes a first region of n-type silicon carbide 64 formed on the p-type base layer 14 adjacent a surface opposite the n-type silicon carbide drift layer 12 to provide an emitter region for the bipolar transistor of  
15 the MOS-bipolar transistor 200. This first region of n-type silicon carbide 64 is preferably doped to have a higher carrier concentration than the n-type conductivity layer 12 so as to provide a first region 64 of n<sup>+</sup> silicon carbide. An ohmic contact is also  
20 formed on the first region of n-type silicon carbide 64 so as to provide an emitter contact 28.

An insulating layer 70 is formed on the first layer 12 adjacent to and disposed from the sidewall of the mesa 82. An ohmic contact is formed on the  
25 insulating layer 70 to provide a gate contact 72 for the MOS transistor. This insulator layer 70 is preferably an oxide layer such as silicon dioxide, but may also be made of other materials such as silicon nitride, aluminum nitride or other insulator materials  
30 known to those of skill in the art.

The MOS-bipolar transistor 200 also includes a second region of n<sup>+</sup> silicon carbide 206 formed in the n<sup>-</sup> drift layer 12 at the base of the sidewall of mesa 282 and extends from the sidewall to beneath a gate  
35 contact 72 of the device. The second region of n<sup>+</sup> silicon carbide 206 preferably is doped to provide a carrier concentration of greater than the n<sup>-</sup> drift layer

12. The second region of n<sup>+</sup> silicon carbide 206 also preferably is formed adjacent the surface of the drift layer 12 so as to allow for contact between the second region of n<sup>+</sup> silicon carbide 206 and conductive strap 92.

Regions of p-type silicon carbide 208 and 90 are also formed in the p-type base layer 14 adjacent second region of n<sup>+</sup> silicon carbide 206 and in the p-type base layer 14 at the step 284 in the mesa 282.

10 The p-type region of silicon carbide 208 extends into the n-type drift layer 12 below the second region of n<sup>+</sup> silicon carbide 206 and below the gate contact 72. The p-type regions of silicon carbide 208 and 90 are preferably doped to provide a carrier concentration

15 greater than the carrier concentration of the p-type base layer 14. Furthermore, the p-type region of silicon carbide 90 is formed so as to convert electrons flowing through the second region of n<sup>+</sup> silicon carbide 206 into holes for injection in the p-type base layer.

20 The p-type region of silicon carbide 208 is formed so as to reduce the field crowding associated with the gate insulator 70 to thereby increase the blocking voltage of the MOS transistor portion of the MOS-bipolar transistor 200.

25 The MOS-bipolar transistor 200 also includes a conductive strap 92 which electrically connects the second region of n<sup>+</sup> silicon carbide 206 with the p-type region of silicon carbide 90. The conductive strap 92 is preferably formed on an insulating layer 210 which

30 is formed on the sidewall of the mesa 282 and extending to the step portion 284 of the mesa 282. This insulating layer 210 may be an oxide layer. The conductive strap 74 may also connect the second region of n<sup>+</sup> silicon carbide 206 with the p-type region 208 so

35 that the p-type region 208 is at the same potential as the second region of n<sup>+</sup> silicon carbide 206. As is illustrated in Figure 7, the p-type region 208



preferably extends to the exposed surface of the drift layer 12 so that contact may be made between the p-type region 208, the n-type region 206 and the p-type region 90. Thus, the p-type region 208 may be formed so that it is exposed in a region near the base of the mesa 282 and need not extend under the mesa 282. So as to reduced the amount of area required by the device, the distance that the p-type region 208 extends past the base of the mesa 282 is preferably kept to a minimum size which allows for the connections described above.

The p-type base layer 14 preferably has a carrier concentration of from about  $10^{16} \text{ cm}^{-3}$  to about  $10^{18} \text{ cm}^{-3}$  and a thickness of from about  $0.3 \text{ }\mu\text{m}$  to about  $5 \text{ }\mu\text{m}$ . The second n<sup>+</sup> regions 206 are preferably from about  $1 \text{ }\mu\text{m}$  to about  $5 \text{ }\mu\text{m}$  wide and extend under the gate as little as possible but this distance may range from about  $0.5 \text{ }\mu\text{m}$  to about  $3 \text{ }\mu\text{m}$ . The second n<sup>+</sup> regions 206 also preferably extend to a depth of from about  $0.1 \text{ }\mu\text{m}$  to about  $0.5 \text{ }\mu\text{m}$ . Carrier concentrations of greater than about  $10^{18} \text{ cm}^{-3}$  maybe suitable for the n<sup>+</sup> regions 206.

The p<sup>+</sup> regions 208 and 90 are preferably of a thickness of from about  $0.3 \text{ }\mu\text{m}$  to about  $2 \text{ }\mu\text{m}$  with region 208 extending beneath the gate contact 72 from about  $3 \text{ }\mu\text{m}$  to about  $12 \text{ }\mu\text{m}$ . However, the distance which the p<sup>+</sup> region 208 extends beneath the gate contact may vary depending on the particular application. In particular, the space between p<sup>+</sup> regions 208 beneath a gate contact may be utilized to adjust the electric field near the insulating layer 70. As the space between p<sup>+</sup> regions 208 decreases the electric field near the insulating layer 70 may be reduced. Spacings of from about  $1 \text{ }\mu\text{m}$  to about  $5 \text{ }\mu\text{m}$  may be suitable. Carrier concentrations of greater than about  $10^{16} \text{ cm}^{-3}$  are suitable for the p<sup>+</sup> region 208 and 90. Preferably

the doping of the drift layer 12 and p+ region 208 is selected such that the drift layer 12 is completely depleted by the built-in potentials of the p+/n junction and the MOS gate at a zero gate bias.

5           The operation of the embodiments of Figure 5, Figure 6 or Figure 7 is similar to the devices described above with respect to Figures 2 and 3. Both devices provide a silicon carbide device which combines bipolar conduction with MOS gated control.

10       Furthermore, these alternative embodiments also utilize an n-type silicon carbide substrate which allows for referencing the gate voltage to the emitter of the device. These devices also have increased breakdown voltages as the p-type implanted regions in the drift  
15       layer serve to reduce the electric field presented to the gate insulator of the MOS device. Furthermore, because the MOS devices of the alternative embodiments are accumulation mode devices, the electron  
20       accumulation layer mobility of silicon carbide may be exploited. Thus, electron accumulation layer mobilities of about 20 times that the inversion layer carrier mobilities may be achieved. This may provide lower on-state voltage drop in the MOS device.

          Turn on of the devices according to the  
25       present invention is accomplished by the application of a positive bias on the collector 30 (about 3-10 V) and a positive bias on the gate 72 (about 15-40 V) while the emitter 28 is kept at ground potential. The source of the NMOSFET 66, 86 and 206 is floating during the  
30       off state and is at approximately 3 V (the silicon carbide forward bias voltage drop for a p-n junction) above the emitter voltage in operation. A positive bias on the gate 72 enables the turn-on of the nMOSFET. The gate voltage ( $V_g$ ) for turn-on of the device will  
35       then be  $15V + V_t + 3V$ , where  $V_t$  is the threshold voltage for the MOS device. Positively biasing the gate with respect to the source allows a path for the flow of

electrons from the collector to the base of the npn transistor thereby forward biasing its emitter-base junction. The device achieves a high current density operation by the injection of minority carriers into  
5 the low doped drift region by the turn-on of the npn transistor. Hence, this device achieves a high current density with relatively low forward voltage drop. The base current to the npn transistor is limited by the saturation current of the MOS transistor which in turn  
10 results in current saturation characteristics of the LMBT. Higher gate voltage allows for higher base current into the npn transistor and hence a higher saturation current of the LMBT.

The device enters the forward blocking mode  
15 of operation when the gate potential is made the same as the emitter potential. This turns off the NMOSFET which reduces the base current of the npn transistor to zero. After the minority carriers of the npn transistor decay with their characteristic lifetime,  
20 the device stops carrying current and can support substantial collector voltage. This voltage is supported by the p-base 14 to n<sup>-</sup> drift region 12 junction and the p<sup>+</sup> buffer/gate oxide-n<sup>-</sup> drift region junction. The p<sup>+</sup> regions 68, 88 and 208 prevent high  
25 electric fields in the gate dielectric in the forward blocking mode of operation of the device.

The fabrication process of the device of Figure 6 is illustrated in Figures 7A through 7H. As will be appreciated by those of skill in the art in  
30 light of the discussion herein, the fabrication process for the device of Figure 5 is similar to the fabrication process for the device of Figure 6 with the primary difference being the formation of the mesa and corresponding implantations. Furthermore, the  
35 fabrication process for the device of Figure 7 is also similar with the primary difference being the masking location for the n-type and p-type regions.

In fabricating the devices of Figures 5, 6 and 7, as illustrated in Figure 8A, a thick n-type layer 12 is grown on the n<sup>+</sup> substrate 10 utilizing an epitaxial growth process such as that described in the United States Patent No. 4,912,064, the disclosure of which is incorporated herein by reference as if set forth fully. As discussed above, alternatively, an n<sup>+</sup> substrate may be utilized and an n<sup>+</sup> implant performed to provide the n<sup>+</sup> layer 10 and n<sup>+</sup> layer 12. As illustrated in Figure 8B, a second p-type layer 14 is epitaxially grown on the first n-type epitaxially layer 12. The n<sup>+</sup> region 64 is then formed on the p-type layer 14. The n<sup>+</sup> region 64 may be formed by ion implantation or by epitaxial growth.

Figure 8C illustrates the first step in forming a mesa where a mask 100 is formed on the n-type region 64. The mask 100 is formed to a width corresponding to the widest dimension of the upper portion of the mesa 82. The n-type region 64, p-type layer 14 and the mask 100 are then etched to form the upper portion of mesa 82. The mask 100 preferably is formed of a material which etches at a rate similar to the rate of etching of the silicon carbide regions. Thus, a sloped sidewall is formed as the mask 100 etches back to expose portions of the silicon carbide. As will be appreciated by those of skill in the art, the mask 100 may be formed of a photoresist which is then selectively heated so as to achieve the desired resistance to etching. Thus, for example, if the mask 100 etches at the same rate as the silicon carbide, then a sloped sidewall of about 45 degrees will be formed. The sloped sidewalls may be etched utilizing the reactive ion etching techniques described in United States Patent No. 4,981,551, the disclosure of which is incorporated herein by reference as if set forth fully.

Figure 8D illustrates the formation of a second mask 102 which is formed on the first mesa which

results from etching the masked region of Figure 8C. As with the mask 100 of Figure 8C, the mask 102 of Figure 8D is sized so as to define the maximum width of the base of the mesa 82 and to provide the step portion 84. The structure of Figure 8D is then etched such that the mesa 82 is completed where the etching process etches the mask 102 and etches through p-type layer 14 to the drift layer 12. As with mask 100, mask 102 may be a photoresist wherein the rate at which the photoresist etches in relation to the rate that silicon carbide is controlled so as to provide a sloped sidewall to the mesa 82.

As is illustrated in Figure 8E, the p-type regions 88 and 90 may be formed by ion implantation utilizing a third mask 104. The mask 104 is preferably formed so as to position the p-type region 88 beneath the gate of the device and so that the p-type region 88 extends to the p-type layer 14. The mask 104 is also preferably formed so as to position the p-type region 90 at the step portion 84 of the mesa 82. The p-implanted regions 88 and 90 may be formed by a method such as those described in United States Patent No. 5,087,576, the disclosure of which is incorporated herein by reference as if set forth fully.

After formation of the p-type regions 88 and 90, as is seen in Figure 8F, the mask 104 is removed and a fourth mask 106 is formed for formation of the n-type regions 86. Mask 106 is preferably formed so as to position the n-type regions 86 to extend from the p-type region to the gate of the device. The n-type regions 86 are then formed by ion implantation using the mask 106. After formation of the n-type regions 86 and the p-type regions 88 and 90, the structure is annealed, preferably at a temperature greater than about 1500 °C to activate the implanted ions.

After annealing, the device may be edge terminated by etching an isolation mesa surrounding the

device. The isolation mesa (not shown) may extend through the second layer 14 and the first layer 12 and into the substrate 10. Alternatively, the isolation mesa may extend through the second layer 14 and into the first layer 12. In such a case, ions may be implanted in the exposed n<sup>-</sup> layer 12 to a depth of from about 100 Å to about 5 μm and to a distance of from about 5 μm to about 500 μm from the edge of the isolation mesa. Carrier concentrations of from about  $5 \times 10^{15} \text{ cm}^{-3}$  to about  $1 \times 10^{17} \text{ cm}^{-3}$  may be utilized to form a low doped p-type region surrounding the isolation mesa.

After formation of the mesa 82 and the n-type and p-type regions 86, 88 and 90, an insulator/oxide layer 70 is formed on the epitaxial structure as illustrated in Figure 8G. The insulator/oxide layer 70 preferably utilizes either a thermal oxidation process such as that described in commonly assigned United States Patent Application Serial No. 08/554,319 entitled "Process For Reducing Defects In Oxide Layers In Silicon Carbide", the disclosure of which is incorporated herein by reference as if set forth fully, or a deposited oxide process such as that described in United States Patent No. 5,459,107 and United States Patent Application Serial No. 08/554,319, the disclosures of which are incorporated herein by reference as if set forth fully. If the thermal oxidation process is used then the preferred embodiment is to use carbon faced wafers such as described in United States Patent No. 5,506,421, the disclosure of which is incorporated herein by reference as if set forth fully.

After formation of the insulator/oxide layer 70, the layer is then etched to provide openings for the formation of the conductive strap 92, gate contact 72 and emitter contact 28. The formation of contacts for the present device is illustrated in Figure 8H.

The gate contact may be formed by depositing a conducting layer on the insulator/oxide layer 70 and then patterning this conductive layer. As illustrated in Figure 8H the gate material 72, preferably molybdenum, may be deposited on the insulating layer 70 and patterned so as to extend above a portion of the n-type region 86. The emitter contact 28 and the optional conductive strap 34 may be formed simultaneously by forming openings in the insulating layer 70 and then depositing nickel or other suitable contact materials on the exposed portions of layers 14 and 12. Finally, a collector contact 30 is formed on the exposed side of the substrate by deposition of nickel or other suitable contact material.

In each of the embodiments described above with respect to Figures 5 through 8H, the substrate and layers may be formed of silicon carbide selected from the group of 6H, 4H, 15R, or 3C silicon carbide, however, 4H silicon carbide is preferred for each of the devices described above. The preferred metals for ohmic contacts include nickel, tantalum silicide and platinum. Additionally, aluminum/titanium contacts may also be used to form the ohmic contacts of the present invention. While these particular metals have been described, any other metals known to those of skill in the art which form ohmic contacts with silicon carbide may be used.

With regard to the carrier concentrations or doping levels of the epitaxial layers and implanted regions of the devices described above, the p' or n' conductivity type regions and epitaxial layers should be as heavily doped as possible without causing excessive fabrication defects. Suitable dopants for producing the p-type regions include aluminum, boron or gallium. Suitable dopants for producing the n-type regions include nitrogen and phosphorus. Aluminum is the preferred dopant for the p' regions and it is

preferred that the aluminum be implanted in the p' regions using high temperature ion implantation such as is described above and employing temperatures of between about 1000°C and about 1500°C and preferably greater than about 1500°C. Carrier concentrations of up to about  $3 \times 10^{17} \text{ cm}^{-3}$  are suitable for the n epitaxial layers, however, carrier concentrations of about  $3 \times 10^{16} \text{ cm}^{-3}$  or less are preferred.

As will be appreciated by those of skill in the art, the thickness of epitaxial layers 12 and 14 will be dependent upon the desired operating characteristics of the device. Furthermore, these operating characteristics will be affected by the number of unit cells employed and the geometry of the unit cells in a multiple cell device. The width of the gate will also be dependent upon the desired operating characteristics of the device, the number of unit cells employed to achieve those operating characteristics, and the geometry utilized for the unit cell itself.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.



## CLAIMS:

1. A MOS bipolar transistor comprising:  
a silicon carbide npn bipolar transistor on a  
bulk single crystal n-type silicon carbide substrate  
5 and having an n-type drift layer and a p-type base  
layer;  
a silicon carbide nMOSFET in said p-type base  
layer including spaced apart n-type source and drain  
regions with a gate region therebetween and adjacent  
10 said npn bipolar transistor so as to provide base  
current to said npn bipolar transistor when said  
bipolar transistor is in a conductive state; and  
means for converting electron current flowing  
between said source and said drain into hole current  
15 for injection into said p-type base layer.
2. A MOS bipolar transistor according to  
Claim 1, wherein said means for converting comprises a  
silicon carbide tunnel diode in said p-type base layer  
20 between said nMOSFET and said npn bipolar transistor so  
as to convert electron current flowing through said  
nMOSFET to hole current for injection into said base  
layer of said npn bipolar transistor.
- 25 3. A MOS bipolar transistor according to  
Claim 2, wherein said tunnel diode includes a region of  
p-type conductivity silicon carbide having a higher  
carrier concentration than said p-type base layer  
adjacent said n-type conductivity source region so as  
30 to provide a conductive p-n tunnel junction between  
said source region and said p-type conductivity region.
4. A MOS bipolar transistor according to  
any of the preceding claims wherein said silicon  
carbide nMOSFET comprises a UMOSFET having a gate  
35 trench adjacent said npn bipolar transistor and having  
a source region so as to provide electrons to said

means for converting and wherein said npn bipolar transistor comprises a vertical npn bipolar transistor.

5. A MOS bipolar transistor according to Claim 1, wherein said p-type base layer forms a mesa on  
5 said n-type drift layer.

6. A MOS bipolar transistor according to Claim 5, wherein sidewalls of said mesa includes a step portion and wherein said means for converting comprises:

10 a region of p-type conductivity silicon carbide in said p-type base layer at said step portion having a higher carrier concentration than said p-type base layer; and

an electrically conductive strap for  
15 electrically connecting the n-type source region of said nMOSFET to said region of p-type conductivity silicon carbide.

7. A MOS bipolar transistor according to any of Claims 5 or 6, wherein said mesa has sloped  
20 sidewalls wherein the slope of the sidewalls provides a predefined doping profile associated with said means for reducing field crowding.

8. A MOS bipolar transistor according to any of the preceding claims, wherein said nMOSFET is an  
25 accumulation mode nMOSFET.

9. A MOS bipolar according to any of the preceding claims further comprising means for reducing field crowding associated with an insulating layer of said nMOSFET.

30 10. A MOS bipolar transistor according to any of the preceding claims wherein said means for

converting comprises:

a region of p-type conductivity silicon carbide in said p-type base layer and having a higher carrier concentration than said p-type base layer; and

5 an electrically conductive strap for electrically connecting the n-type source region of said nMOSFET to said region of p-type conductivity silicon carbide.

11. A MOS bipolar transistor according to  
10 any of the preceding claims, wherein said MOS bipolar transistor includes a plurality of unit cells so as to provide a plurality of electrically parallel npn bipolar transistors.

12. A MOS bipolar transistor according to  
15 any of the preceding claims, wherein said MOS bipolar transistor is formed on a 4H n-type conductivity bulk single crystal silicon carbide substrate.

13. A unit cell of a MOS bipolar transistor  
20 comprising:

an n-type bulk single crystal silicon carbide substrate;

an n-type silicon carbide drift layer  
adjacent said n-type conductivity bulk single crystal  
25 silicon carbide substrate, said n-type drift layer having a carrier concentration of less than said n-type silicon carbide substrate;

a p-type silicon carbide base layer on said  
n-type silicon carbide drift layer;

30 a first n-type region of silicon carbide in said p-type base layer;

a gate trench in said p-type base layer and extending through said base layer and said first n-type region to said drift layer so as to provide a portion

of said n-type region as a portion of the sidewall of said gate trench;

an insulating layer on the bottom and sidewalls of said gate trench;

5 a second n-type conductivity region of silicon carbide in said base layer adjacent and disposed from said gate trench;

a gate contact on said insulating layer and extending over a portion of said first n-type region;

10 a collector contact on a surface of said silicon carbide substrate opposite said drift layer;

a p-type region of silicon carbide in said base layer and disposed between said first n-type region and said second n-type region, said p-type region having a carrier concentration greater than the carrier concentration of said p-type base layer and formed so as to convert electrons flowing through said first n-type region into holes for injection into said p-type base layer; and

20 an emitter contact on said second n-type region of silicon carbide.

14. The unit cell according to Claim 13, further comprising:

25 a p-type region of silicon carbide in said n-type silicon carbide drift region at the bottom of said gate trench and having a carrier concentration greater than the carrier concentration of said p-type base layer.

30 15. The unit cell according to any of Claims 13 or 14, wherein said p-type region forms a p-n junction with said first n-type region so as to provide a tunnel diode.

16. The unit cell according to any of Claims 13, 14 or 15, further comprising:

a conductive strap between said first n-type region and said p-type region so as to provide electrical connection between said p-type region to said first n-type region.

5

17. A unit cell of a MOS bipolar transistor comprising:

an n-type bulk single crystal silicon carbide substrate;

10

an n-type silicon carbide drift layer adjacent said n-type conductivity bulk single crystal silicon carbide substrate, said n-type drift layer having a carrier concentration of less than said n-type silicon carbide substrate;

15

a p-type epitaxial silicon carbide base layer formed on said n-type silicon carbide drift layer;

a first n-type region of silicon carbide formed in said p-type base layer adjacent a surface opposite said n-type silicon carbide drift layer;

20

wherein said p-type epitaxial silicon carbide base layer is formed as a mesa having a sidewall which extends through said p-type epitaxial silicon carbide base layer and to said n-type drift layer;

an insulating layer formed on said n-type drift layer adjacent and disposed from said sidewall;

25

a second n-type conductivity region of silicon carbide formed in said drift layer adjacent said sidewalls of said mesa, said second-n-type conductivity region having a higher carrier

concentration than said drift layer;

30

a gate contact on said insulating layer and extending over a portion of said first n-type region;

a collector contact on a surface of said silicon carbide substrate opposite said drift layer;

35

a first p-type region of silicon carbide in said base layer and a second p-type region form adjacent said second n-type conductivity region and

- extending into said n-type drift region below said second n-type conductivity region and below said gate contact, said first and second p-type regions being electrically connected and having a carrier concentration greater than the carrier concentration of said p-type epitaxial base layer and said first p-type region being formed so as to convert electrons flowing through said first n-type region into holes for injection into said p-type base layer;
- 5 a conductive strap formed at base of said sidewall so as to electrically connect said second n-type conductivity region with said first p-type region of silicon carbide; and
- 10 an emitter contact on said first n-type region of silicon carbide.
- 15

18. The unit cell according to Claim 17 wherein the first and second regions of p-type silicon carbide comprise a continuous region of p-type silicon carbide formed in said base layer adjacent a sidewall of said mesa and said second n-type conductivity region and extending into and below said gate contact.

20

19. The unit cell according to any of Claims 17 or 18, wherein the sidewall has a slope of less than about 60 degrees.

20. The unit cell according to any of Claims 17, 18 or 19, wherein the slope of the sidewall is selected so as to produce said second p-type regions of silicon carbide when p-type ions are implanted at a predetermined depth in said drift layer.

25

21. The unit cell according to any of claims 17, 18, 19 or 20, wherein said sidewall comprises two sidewalls so as to provide a step in the sidewall of said mesa;

30

wherein said first and second p-type regions of silicon carbide comprise:

a first p-type region of silicon carbide formed in said p-type epitaxial base layer adjacent  
5 said step; and

a second p-type region of silicon carbide formed in said n-type drift layer adjacent said second n-type conductivity region, extending into said n-type drift layer below said gate contact and extending to  
10 said p-type base layer.

22. The unit cell according to Claim 21, wherein said second p-type region is formed so as to be exposed at a surface of if said drift layer and wherein said conductive strap electrically connects said first  
15 p-type region with said second p-type region and said second n-type region.

23. The unit cell according to Claim 22, further comprising an insulating layer formed on the sidewall of said mesa between said drift layer and said  
20 step and extending onto said step and wherein said conducting strap is formed on said insulating layer.

24. A unit cell according to any of Claims 17 through 23, wherein said second p-type region extends beneath the gate contact a distance of from  
25 about 3  $\mu\text{m}$  to about 12  $\mu\text{m}$ .

25. A unit cell according to any of Claims 17 through 24, wherein the second n-type conductivity region extends into the n-type drift layer to a depth of from about 0.3  $\mu\text{m}$  to about 5  $\mu\text{m}$ .

30 26. The unit cell according to any of Claims 13 through 25, wherein said p-type base layer has a thickness of from about 0.3  $\mu\text{m}$  to about 5  $\mu\text{m}$ .

27. The unit cell according to any of claims 13 through 26, wherein said n-type drift region has a thickness of from about 3  $\mu\text{m}$  to about 500  $\mu\text{m}$ .

5

28. The unit cell according to any of claims 13 through 27, wherein said n-type drift region has a carrier concentration of from about  $10^{12}$  to about  $10^{17}$   $\text{cm}^{-3}$ .

10

29. The unit cell according to any of claims 13 through 28, wherein said p-type base layer has a carrier concentration of from about  $10^{16}$  to about  $10^{18}$   $\text{cm}^{-3}$ .

15

30. A MOS gated bipolar transistor comprising a plurality of the unit cells of any of claims 13 through 29.

31. A method of forming a MOS bipolar transistor comprising:

20 forming an n-type silicon carbide drift layer on an n-type conductivity bulk single crystal silicon carbide substrate, said n-type drift layer having a carrier concentration of less than said n-type silicon carbide substrate;

25 forming a p-type silicon carbide base layer on said n-type silicon carbide drift layer;

forming a first n-type region of silicon carbide in said p-type base layer;

30 forming a first gate trench formed in said p-type base layer and extending through said base layer and said first n-type region to said drift layer so as to provide a portion of said n-type region as a portion of the sidewall of said gate trench;

forming an insulating layer formed on the bottom and sidewalls of said gate trench;



forming a second n-type conductivity region of silicon carbide formed in said base layer adjacent and disposed from said gate trench;

5 forming a gate contact formed on said insulating layer and extending over a portion of said first n-type region;

forming a collector contact formed on a surface of said silicon carbide substrate opposite said drift layer;

10 forming a p-type region of silicon carbide formed in said base layer and disposed between said first n-type region and said second n-type region, said p-type region having a carrier concentration greater than the carrier concentration of said p-type base layer and formed so as to convert electrons flowing through said first n-type region into holes for injection into said p-type base layer; and

15 forming an emitter contact formed on said second n-type region of silicon carbide.

20

32. The method according to Claim 31, further comprising the step of:

25 forming a p-type region of silicon carbide formed in said n-type silicon carbide drift region at the bottom of said gate trench and having a carrier concentration greater than the carrier concentration of said p-type base layer.

30 33. The method according to any of Claims 31 or 32, wherein said step of forming a p-type region includes the step of forming a p-type region which forms a p-n junction with said first n-type region so as to provide a tunnel diode.

35 34. The method according to Claim 31, further comprising the step of:

forming a conductive strap between said first n-type region and said p-type region so as to provide electrical connection between said p-type region to said first n-type region.

5

35. A method according to Claim 31, further comprising the step of forming a plurality of the unit cells of Claim 18 so as to provide a plurality of electrically parallel MOS gated bipolar transistor.

10

36. A method according to Claim 31, wherein said step of forming an n-type silicon carbide drift layer on an n-type conductivity bulk single crystal silicon carbide substrate comprises the step of

15 implanting ions in a silicon carbide substrate so as to provide a region of higher carrier concentration in the substrate and a drift layer in the substrate.

37. A method of forming a MOS gated bipolar transistor comprising the steps of:

20 forming an n-type silicon carbide drift layer on an n-type bulk single crystal silicon carbide substrate;

forming a p-type silicon carbide base layer

25 on the n-type silicon carbide drift layer;

implanting through a first mask ions so as to form a n-type regions of silicon carbide in the base layer to provide an emitter region and a drain region;

implanting through a second mask ions so as

30 to form a p-type region of silicon carbide adjacent the source region;

etching a trench through a portion of the n-type source region and through the base layer and into the drift layer so as provide a gate trench;

35 forming an insulating layer on exposed surfaces of the base layer and the trench;

forming and patterning an ohmic contact in the trench and on the base layer so as to provide a gate contact;

5 removing a portion of the insulating layer to expose the emitter region formed in the base layer;

forming an emitter contact on the exposed emitter region; and

10 forming a source/emitter contact on a surface of the silicon carbide substrate opposite the drift layer.

38. A method according to Claim 37, wherein said step of implanting through a masking layer is followed by the step of annealing the resultant  
15 structure at a temperature of greater than about 1500 °C.

39. A method according to Claim 37, further comprising the step of forming a p-type silicon carbide  
20 region in the n-type drift layer below the bottom of the trench.

40. A method according to Claim 37, further comprising the steps of:

25 exposing a portion of the n-type source region and the p-type region of higher carrier concentration formed in the base layer;

30 forming on the exposed portion of the n-type source region and p-type region a conductive strap to electrically connect the n-type source region to the p-type region.

41. A method according to Claim 37, wherein said step of implanting ions to form n-type source and emitter regions comprises the step of implanting ions  
35 selected from the group consisting of nitrogen and phosphorus.

42. A method according to Claim 37, wherein  
said step of implanting ions to form a p-type region of  
higher carrier concentration comprises implanting ions  
5 selected from the group consisting of aluminum, boron  
or gallium.

43. A method according to Claim 37, wherein  
said step of forming an n-type silicon carbide drift  
10 layer on an n-type bulk single crystal silicon carbide  
substrate comprises the steps of:

forming an n-type silicon carbide substrate;  
and

15 implanting ions in the silicon carbide  
substrate so as to provide a region of higher carrier  
concentration in the substrate and a drift layer in the  
substrate.

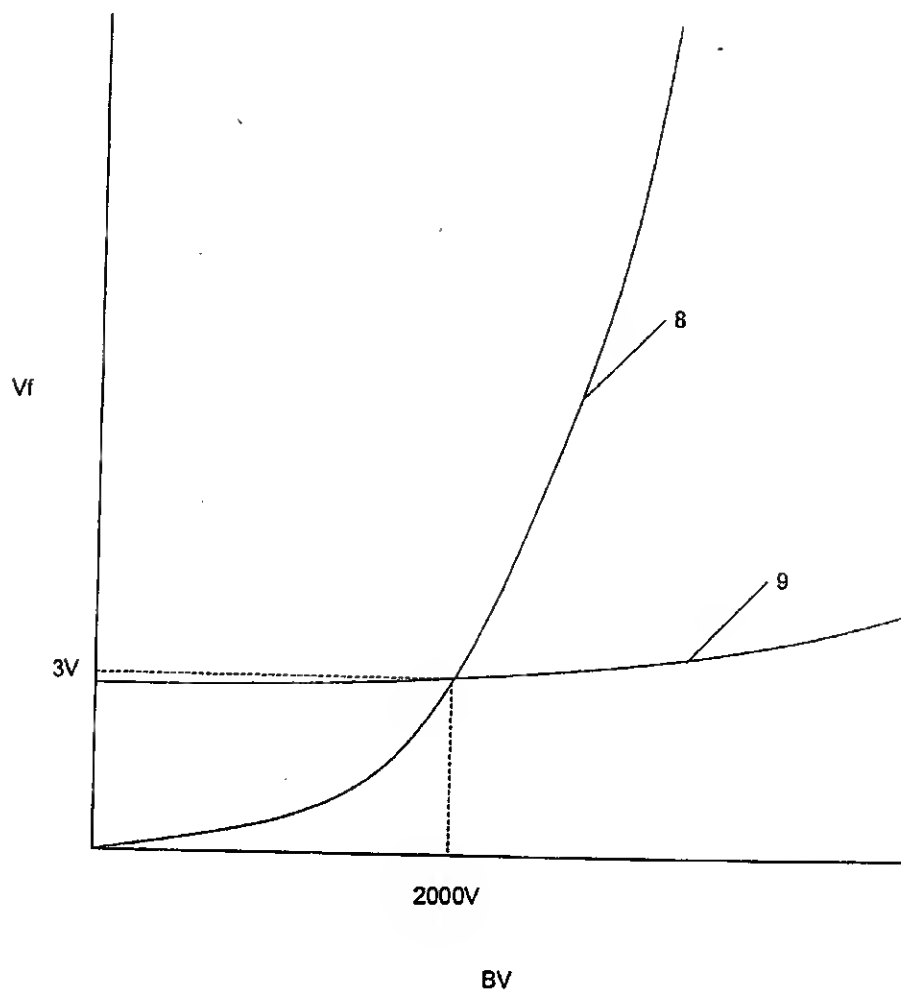


Figure 1

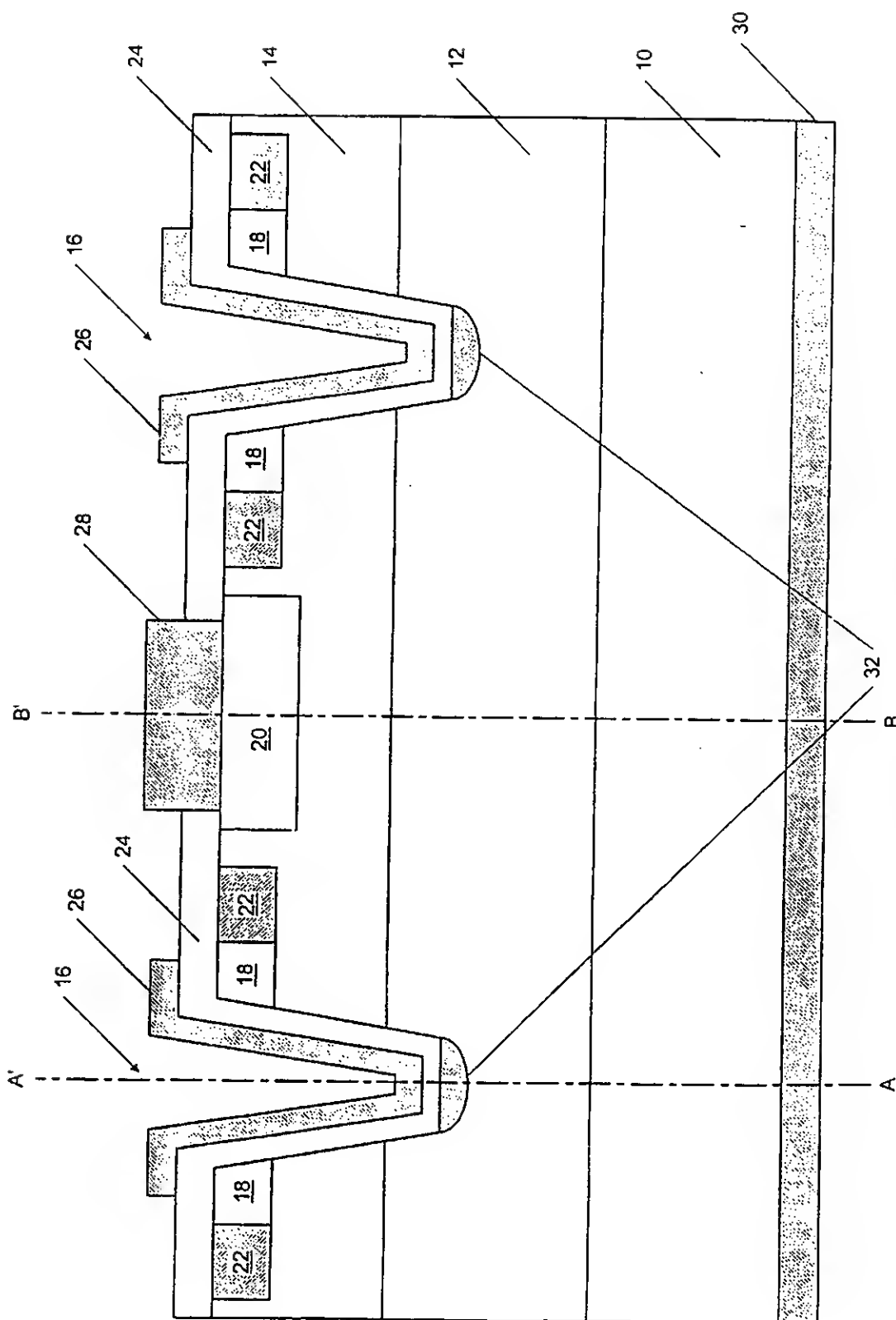


Figure 2

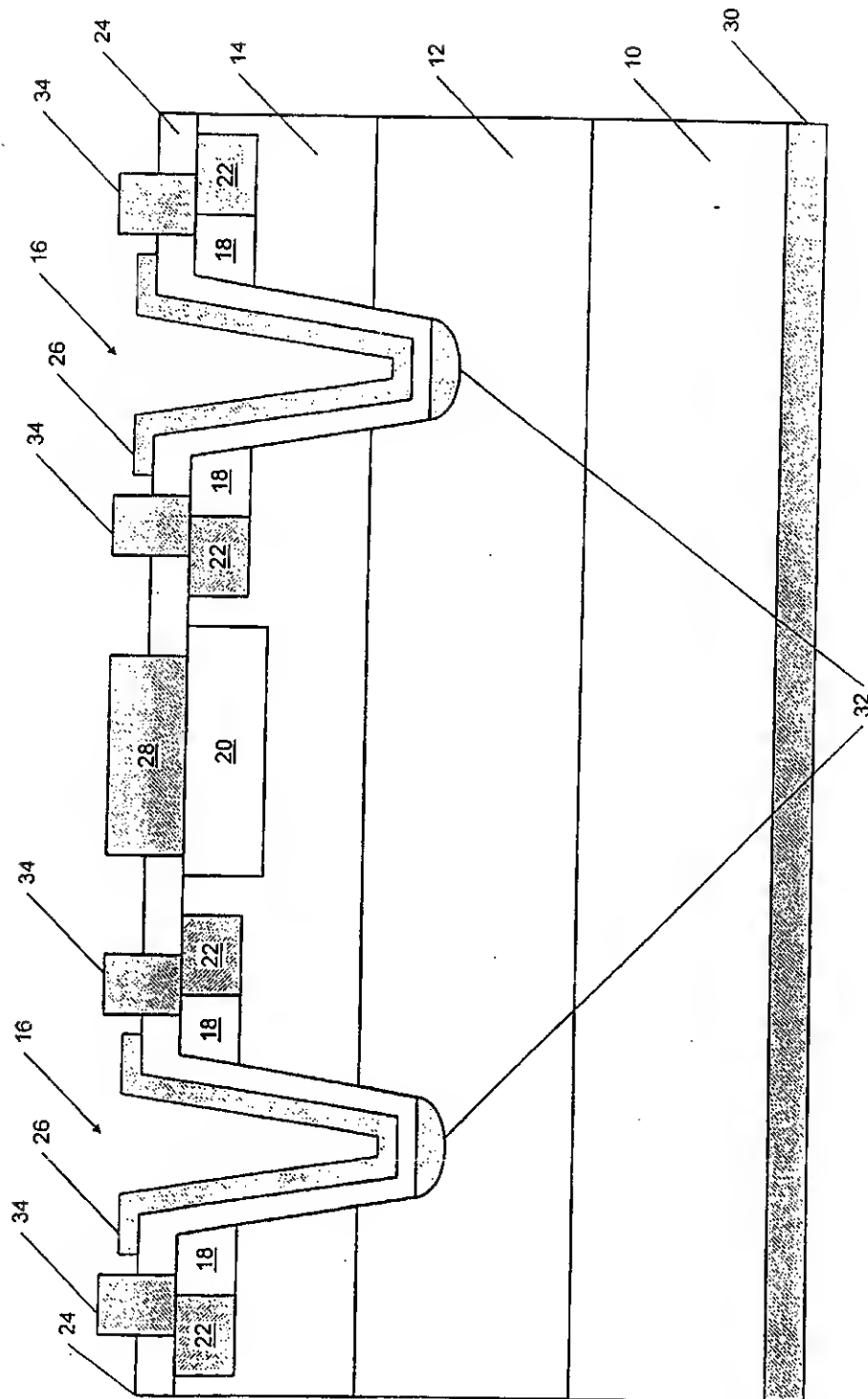


Figure 3

4/18

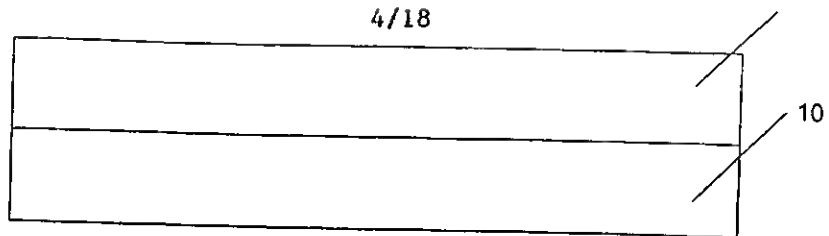


Figure 4A

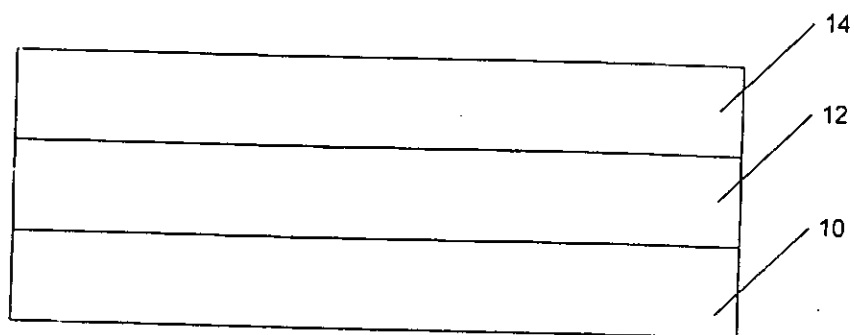


Figure 4B

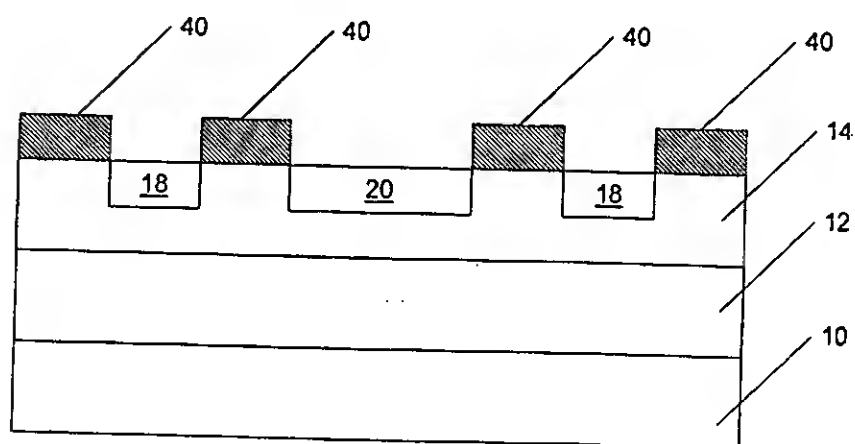


Figure 4C



5/18

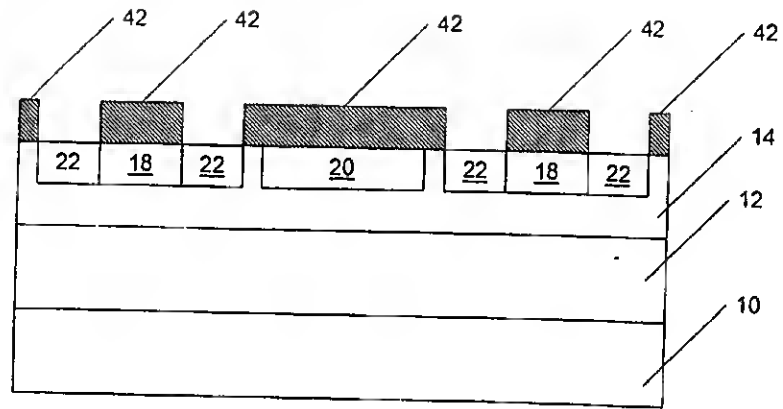


Figure 4D

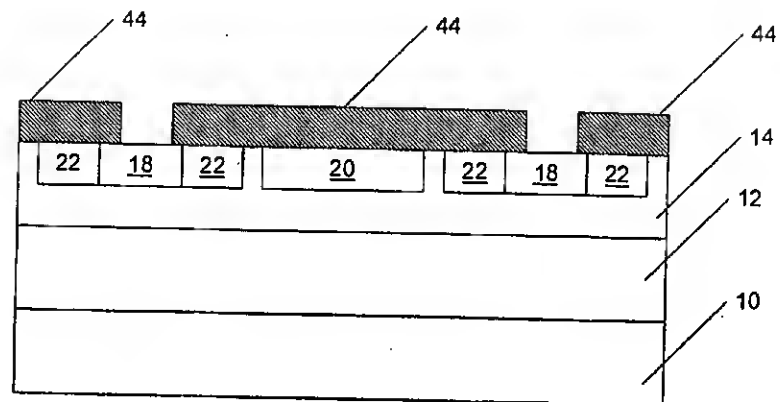


Figure 4E

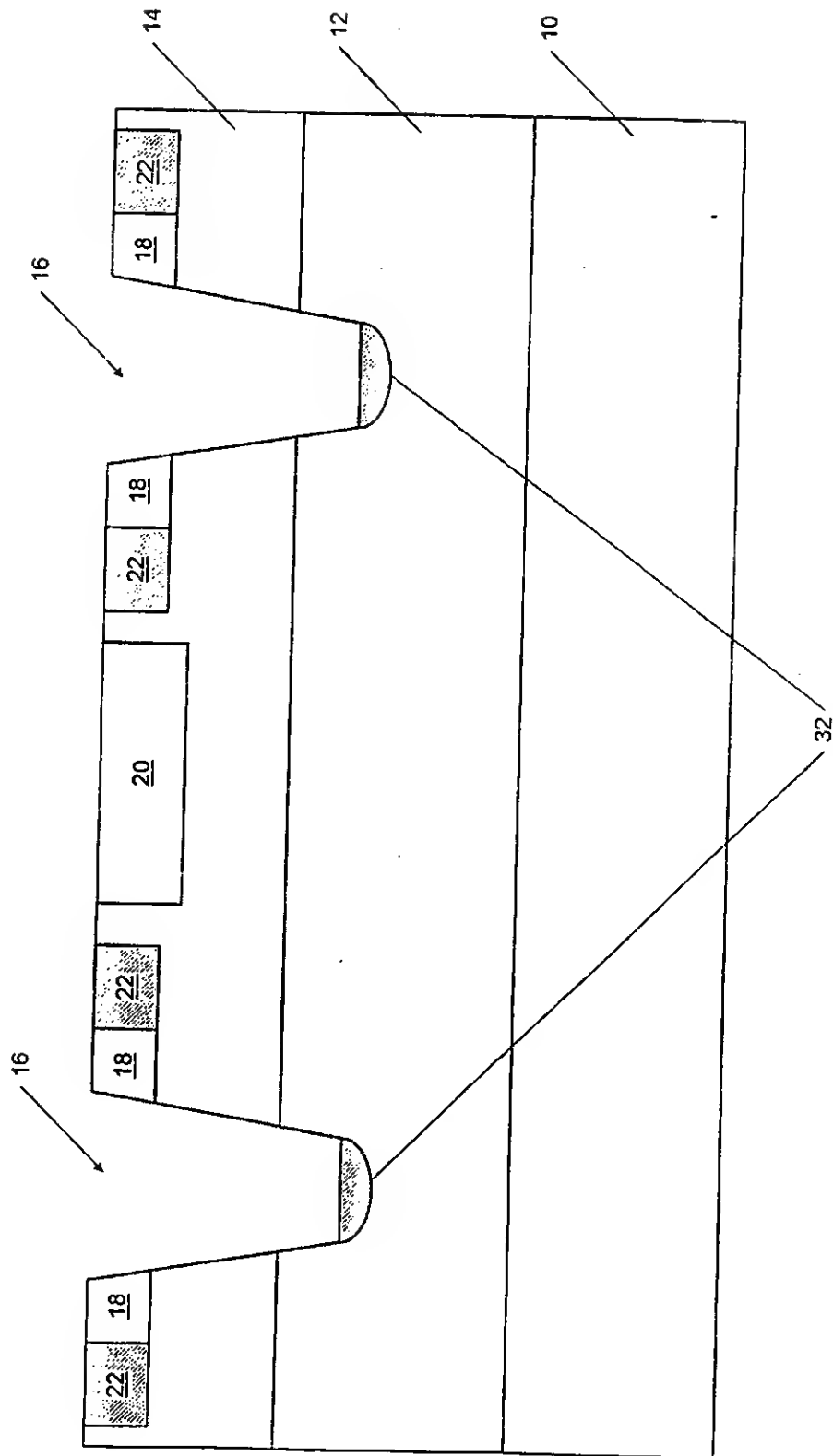


Figure 4F

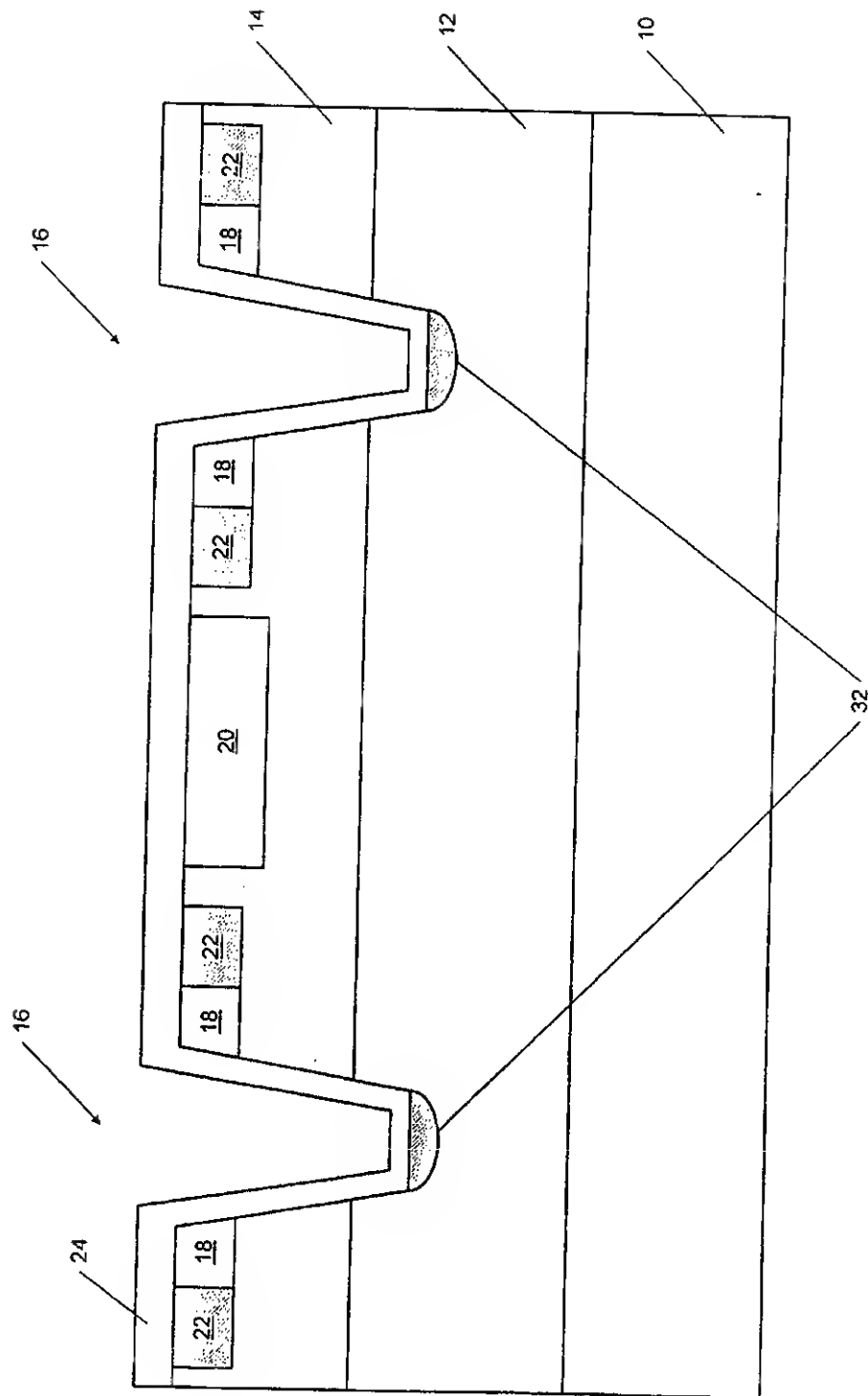


Figure 4G

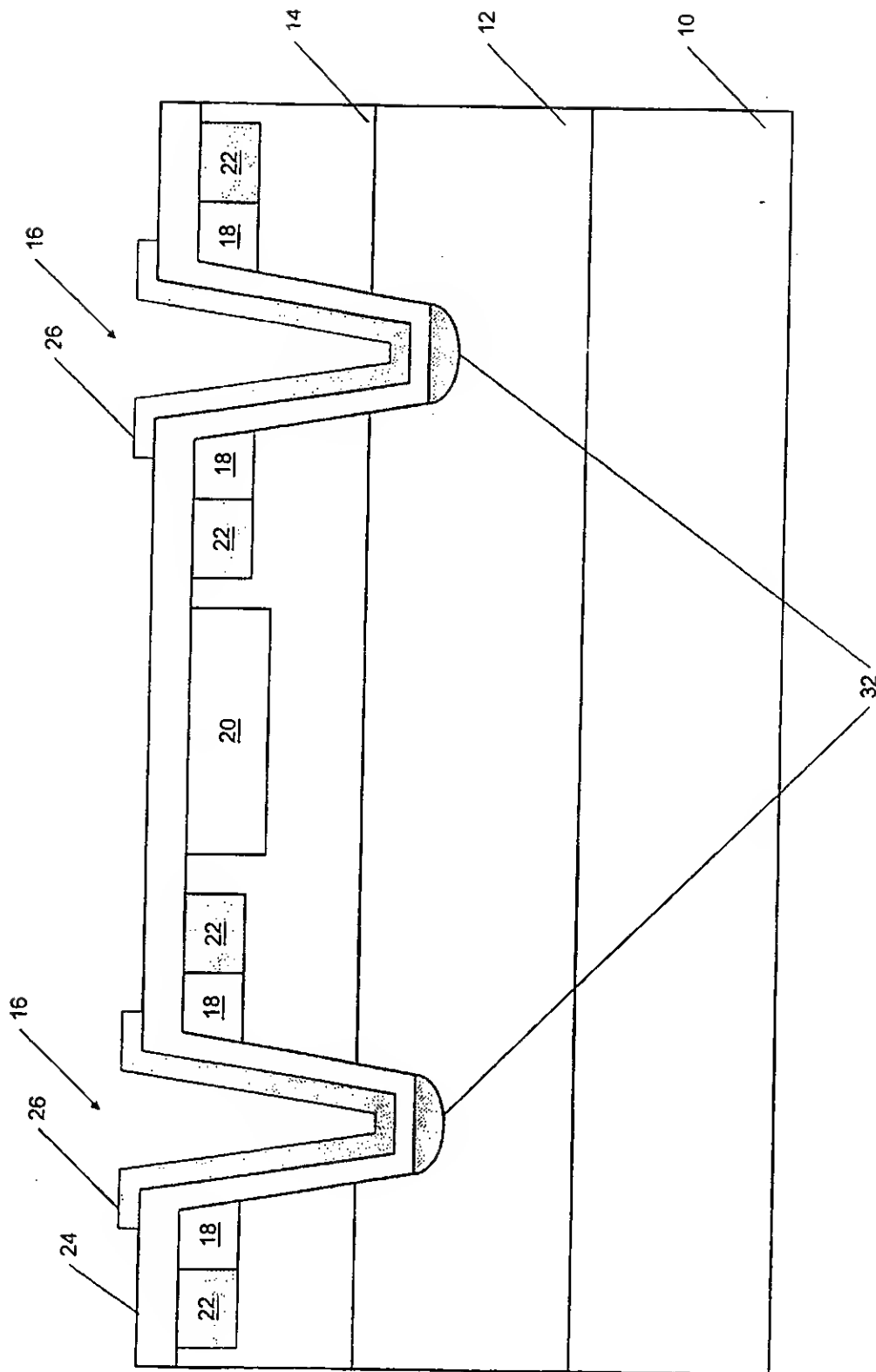


Figure 4H

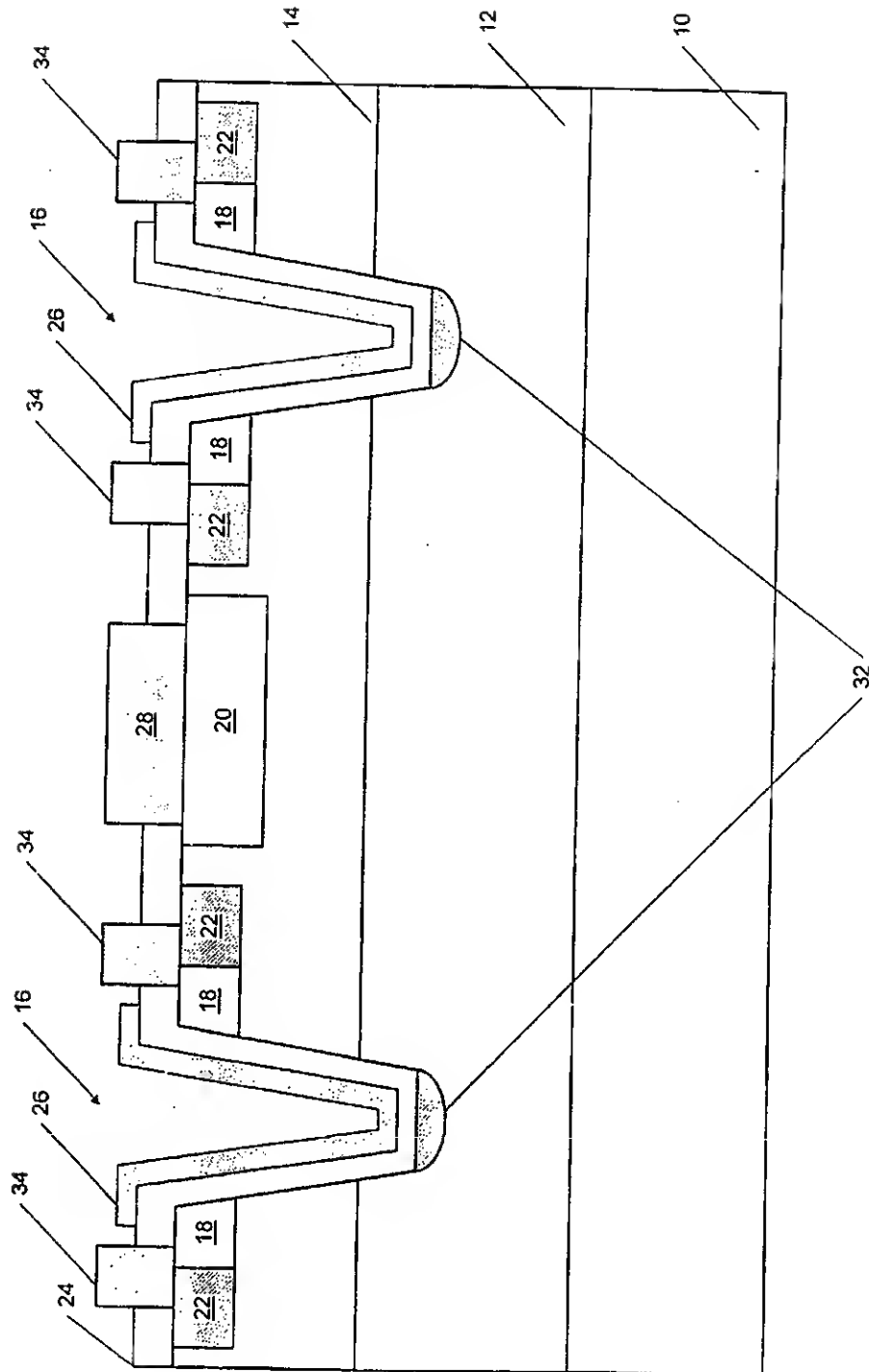


Figure 41

10/18

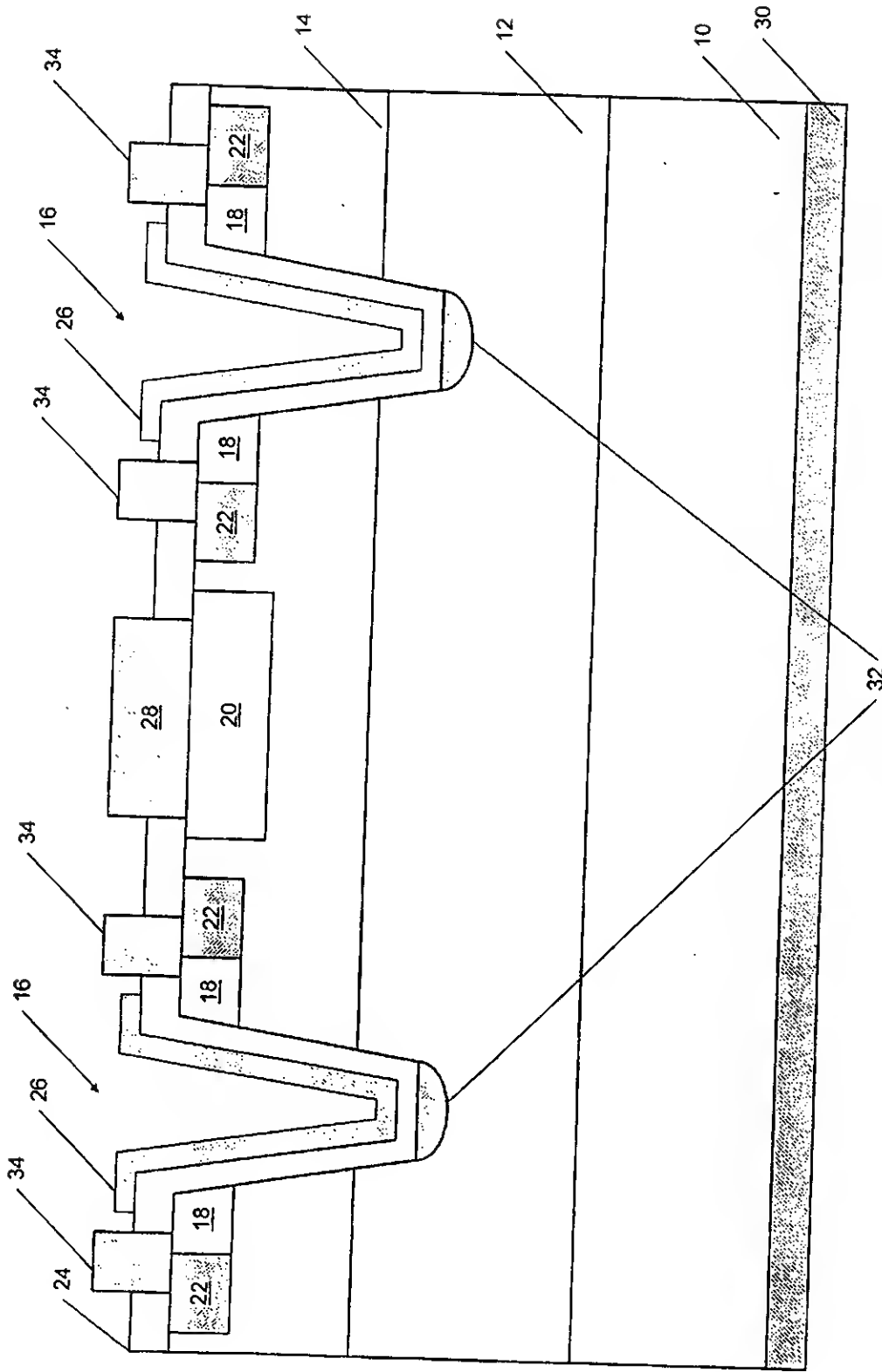


Figure 4J

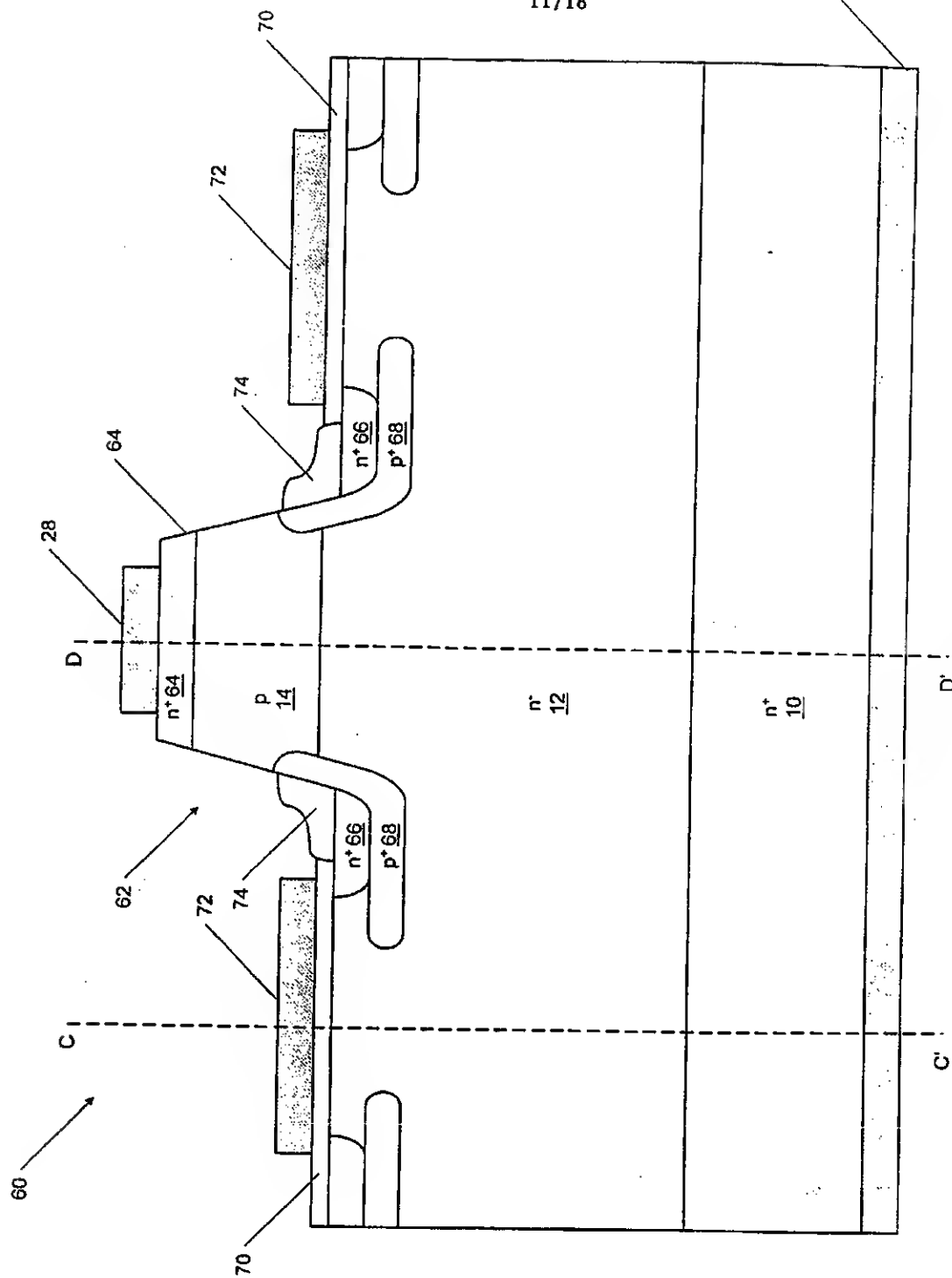


Figure 5

12/18

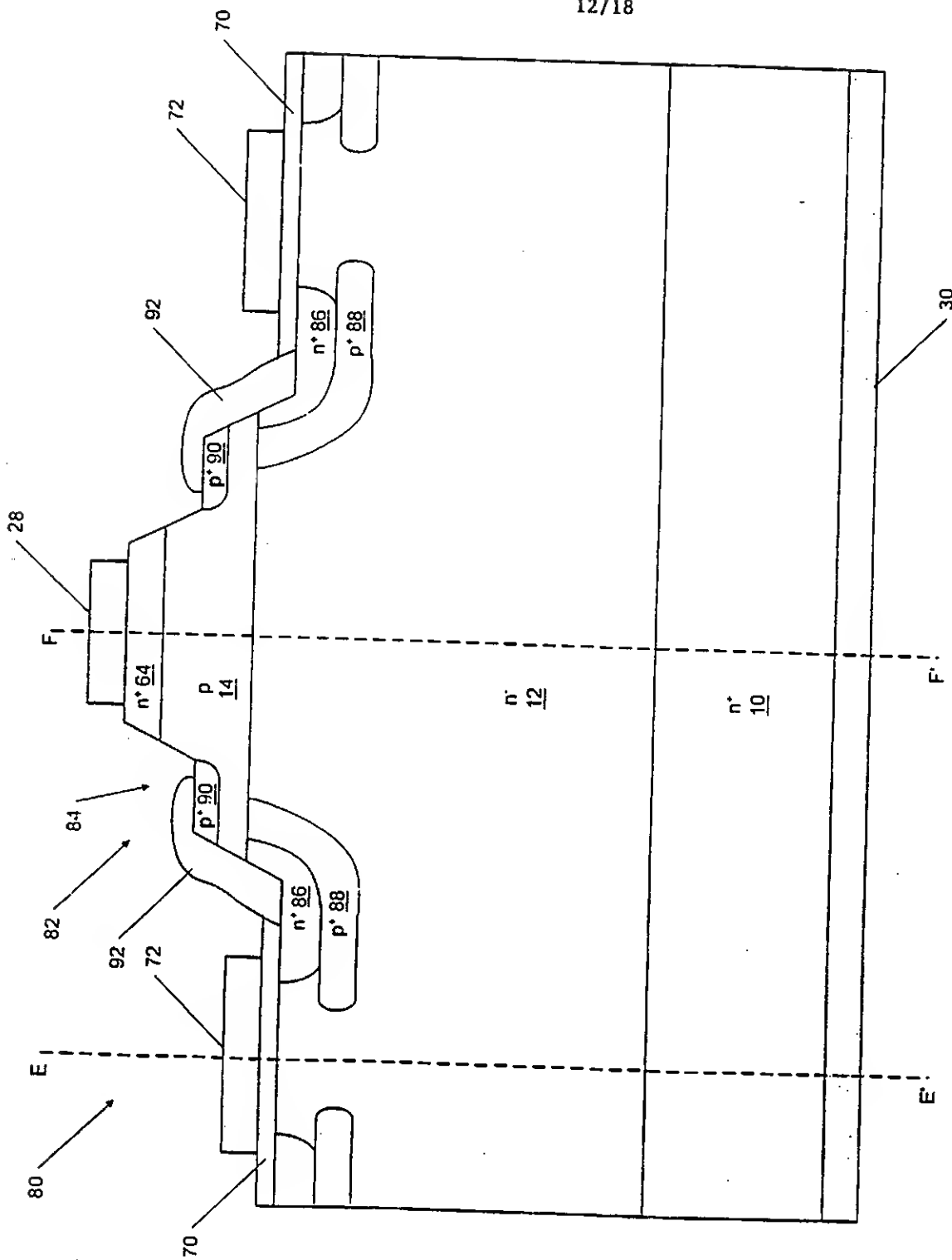


Figure 6



13/18

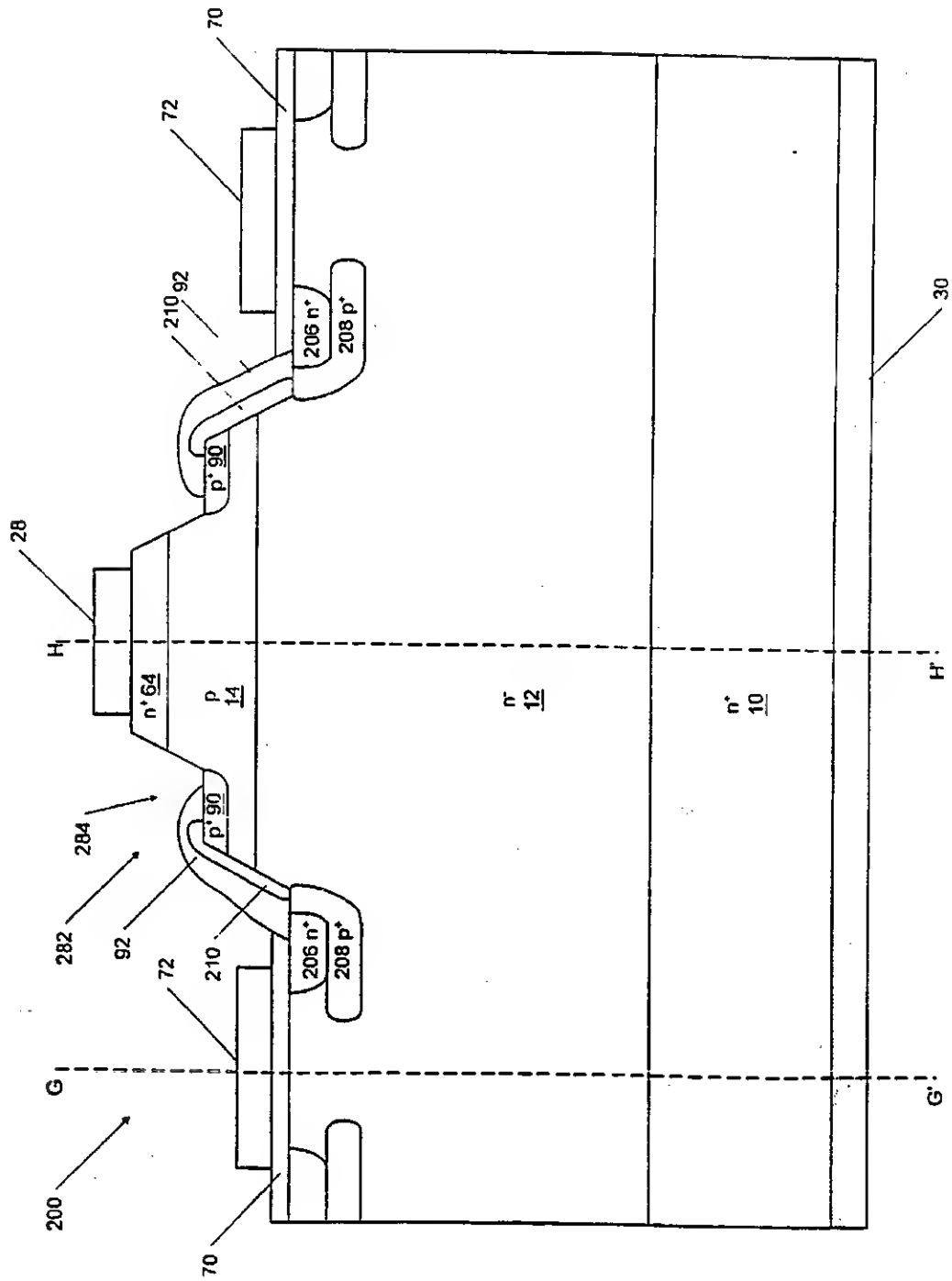


Figure 7

14/18

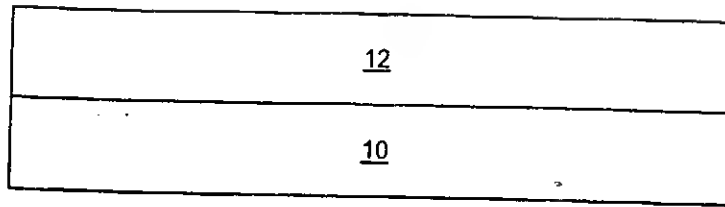


Figure 8A

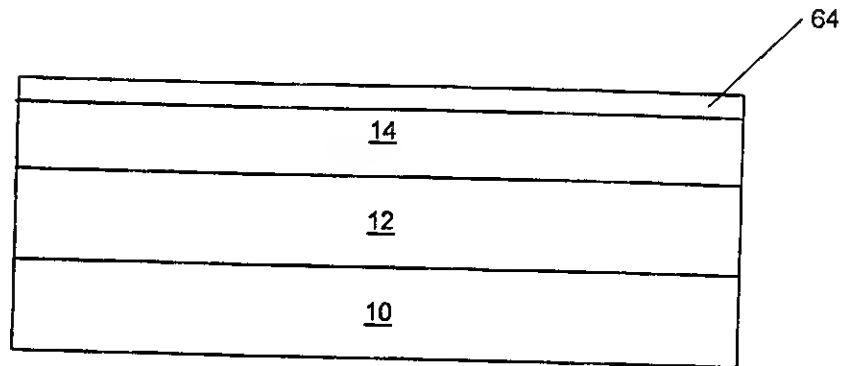


Figure 8B

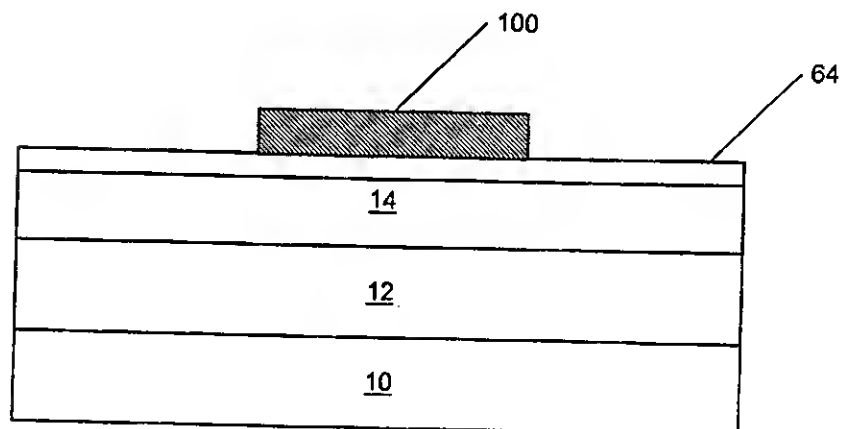


Figure 8C

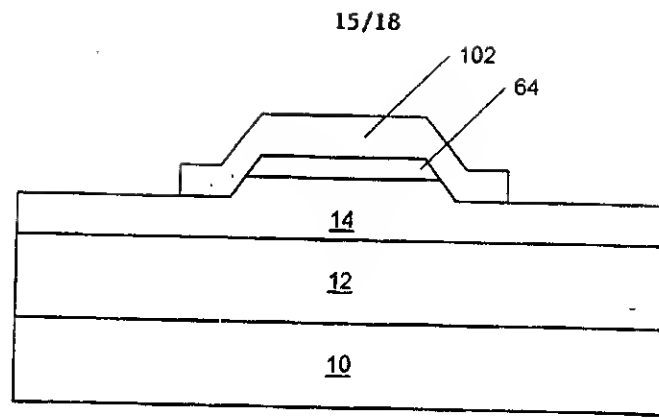


Figure 8D

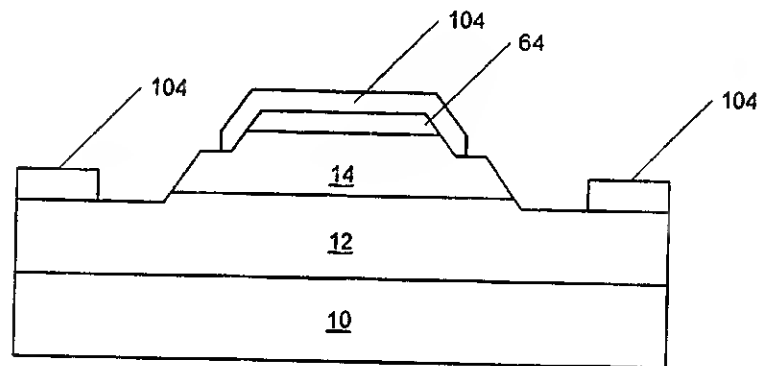


Figure 8E

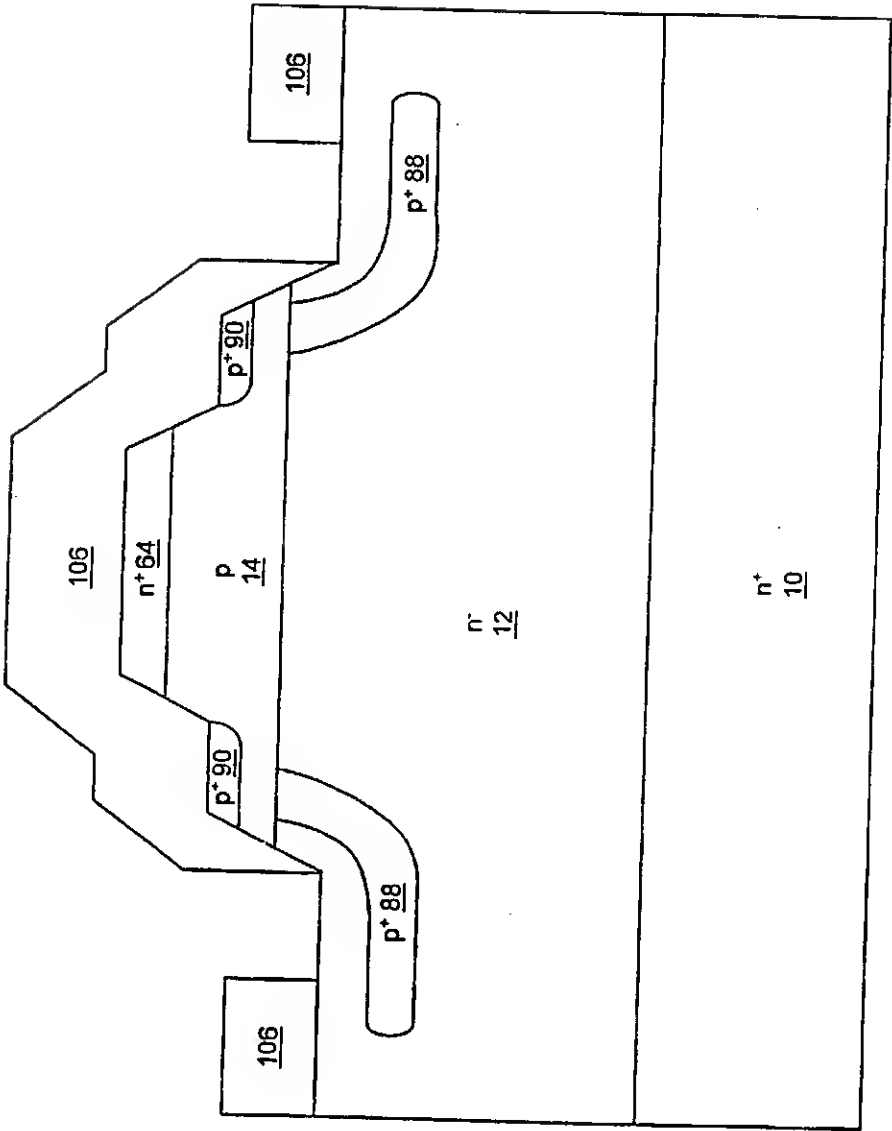


Figure 8F

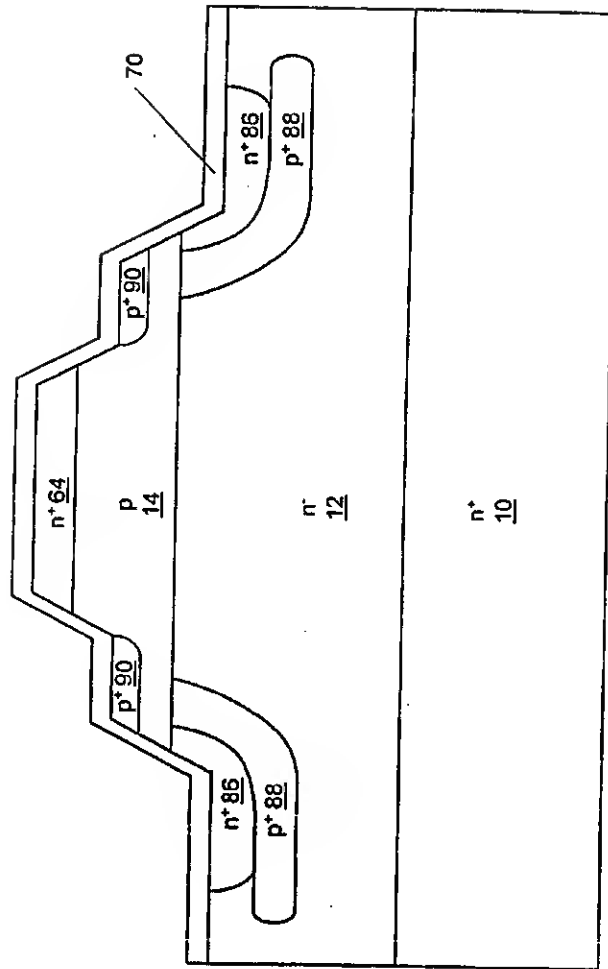


Figure 8G

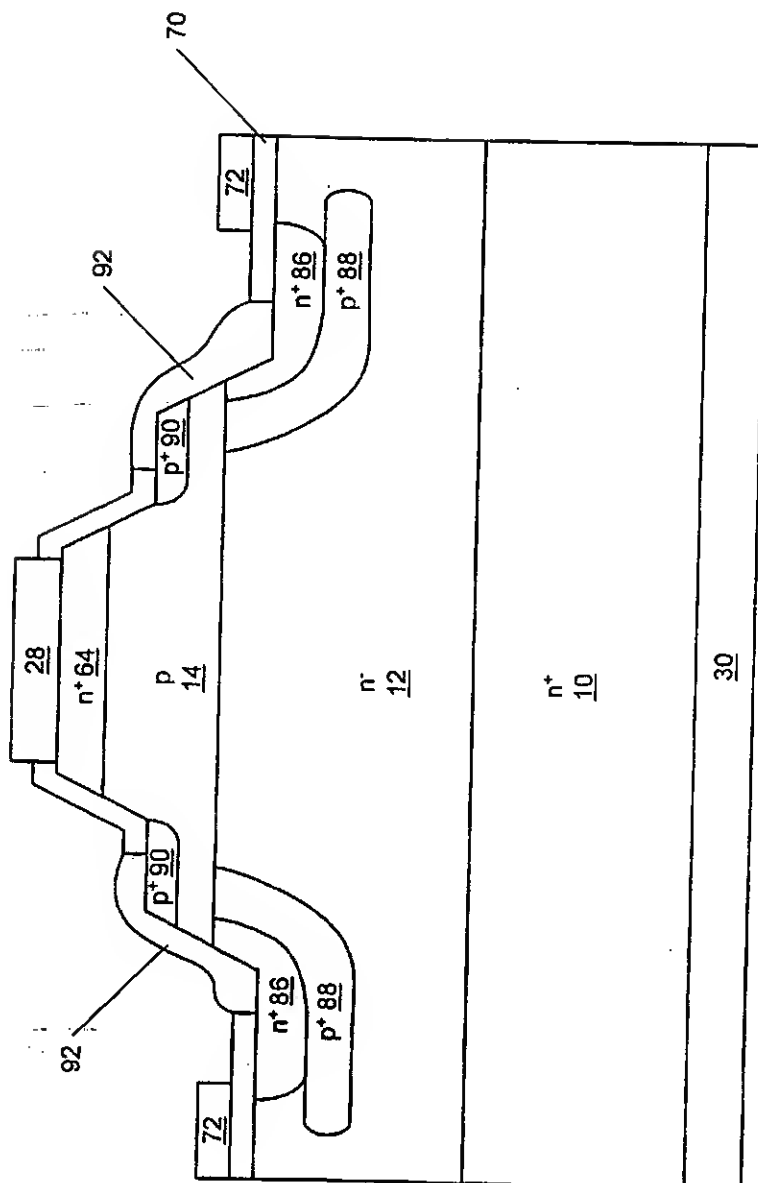


Figure 8H

# INTERNATIONAL SEARCH REPORT

International Application No.  
PCT/US 98/12007

A. CLASSIFICATION OF SUBJECT MATTER  
IPC 6 H01L29/73 H01L29/24

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	FR 2 524 711 A (GEN ELECTRIC) 7 October 1983 see page 22, column 25 - column 34; figure 8 see page 32, column 13 - column 25	1, 4, 6, 8, 15, 16, 37
A	US 4 945 394 A (PALMOUR JOHN W ET AL) 31 July 1990 see abstract; figures	1
X	PARPIA Z ET AL: "A novel CMOS-compatible high-voltage transistor structure", IEEE TRANSACTIONS ON ELECTRON DEVICES, DEC. 1986, USA, VOL. ED-33, NR. 12, PAGE(S) 1948 - 1952, ISSN 0018-9383 XP002077165 see abstract; figure 2	1, 6

-/-

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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- \*O\* document referring to an oral disclosure, use, exhibition or other means
- \*P\* document published prior to the international filing date but later than the priority date claimed

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Date of the actual completion of the international search

16 September 1998

Date of mailing of the international search report

30/09/1998

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## INTERNATIONAL SEARCH REPORT

Inter. Appl. Application No

PCT/US 98/12007

## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication where appropriate, of the relevant passages	Relevant to claim No.
X	E M SANKARA NARAYANAN: "CMOS COMPATIBLE 25D V LATERAL INSULATED BASE TRANSISTORS" 22 Apr 11 1991, PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON POWER SEMICONDUCTOR DEVICES AND IC'S, BALTIMORE, APRIL 22 - 24, 1991, NR. SYMP. 3, PAGE(S) 181 - 186, AYMAN SHIBIB; JAYANT BALIGA XP00021B965 see the whole document	1, 6
X	US 5 331 194 A (UENO KATSUNORI) 19 July 1994 see abstract; figure I	1
A	KENNETH O ET AL: "PMOS INPUT MERGED BIPOLAR/SIDEWALL MOS TRANSISTORS (PBIMOS TRANSISTORS)" 1 February 1991, IEEE ELECTRON DEVICE LETTERS, VOL. 12, NR. 2, PAGE(S) 6B - 70 XP00D165555 see the whole document	1, 4, 5
A	PATENT ABSTRACTS OF JAPAN vol. 01D, no. 285 (E-441), 27 September 1986 -& JP 61 104667 A (OKI ELECTRIC IND CO LTD), 22 May 1986 see abstract	2



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Information on patent family members

International Application No

PCT/US 98/12007

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